Emac API Specification

Feb 26, 2025

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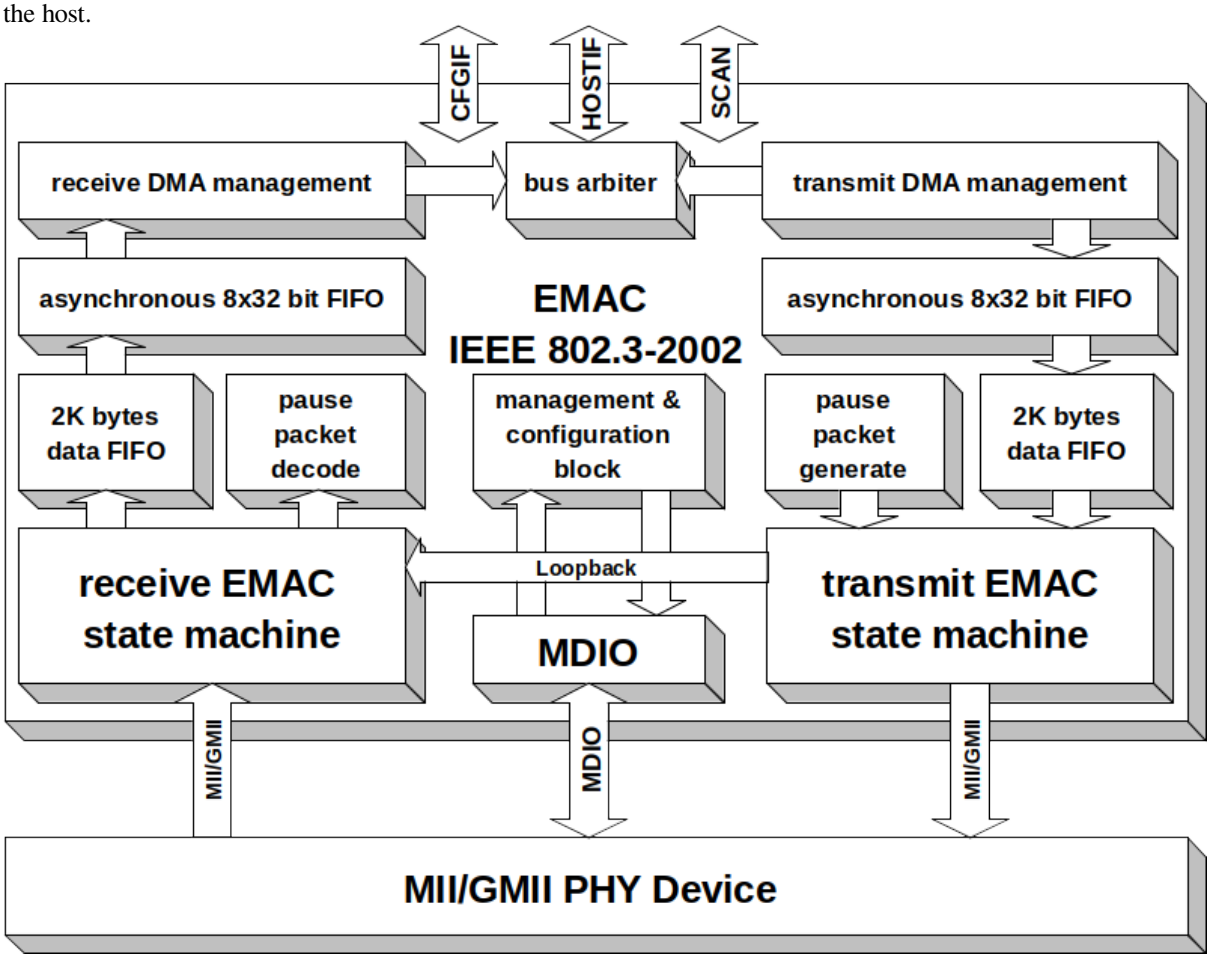
OVERVIEW DOCUMENTATION

CHAPTER
ONE

DESCRIPTION

EMAC is a configurable, fully compatible IEEE 802.3–2002 implementation of Media Access Controller interface operating at 10/100/1000 Mbps with integrated data FIFO's, configuration registers and Tulip DMA host interface. It provides standard MII/GMII and MDIO interfaces to all compliant PHY devices and a generic 32-bit interface to the host.



CHAPTER
TWO

FEATURES

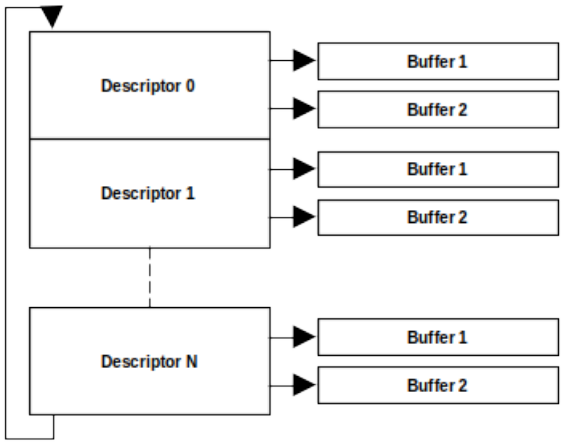
Compatible with the IEEE 802.3–2002 standard
Configurable 10/100/1000 Mbps speed
IEEE Std 802.3-2002 compliant Media Independent Interface for connection to external 10/100 Mbps PHY transceivers
IEEE Std 802.3-2002 compliant Gigabit Media Independent Interface for connection to external 1000 Mbps PHY transceivers
Supports 10BASE-T and 100BASE-TX/FX IEEE Std 802.3-2002 compliant MII PHY's at full or half duplex operating modes
Supports Gigabit Ethernet and 1000BASE-T IEEE Std 802.3-2002 compliant GMII PHY's at full or half duplex operating modes
Supports MDIO management control writes and reads with the PHY's
Configurable Full/Half Duplex for any speed
Supports burst operation and carrier extend when 1000 Mbps operating mode is selected
CSMA/CD compliant operation at 10 Mbps, 100 Mbps, 1000 Mbps in half duplex mode
Pause frame capability IEEE 802.3x compliant
Backpressure half duplex flow control algorithm
Supports Jumbo frame transfer, up to 16KB, both receive and transmit
Configurable address filtering modes: 16 perfect addresses, 512 hash-filtered multicast addresses and one perfect address, inverse perfect filtering
Supports unicast, multicast, and broadcast
Supports promiscuous address receive mode
Provides auto pad and Frame Check Sequence field insertion for transmit operation
Provides auto Frame Check Sequence field checking and removal for receive operation
Programmable interframe gap
Internal FIFO's for TX/RX data flows (configurable size); implemented in Dual port RAM
Internal loop-back capability
32-bit Host interface supporting DMA descriptor base system (Tulip Driver) with one general interrupt line
Configurable DMA transfer burst length
Big/little endian for DMA data transfers
Descriptor/buffer architecture, supporting ring/chain data structures
Automatic descriptor polling
Contains Control and Status Registers Block (CSR)
Provides global and per frame statistics for both transmit and receive
Supports a wide range of Host clock frequencies
Low power capability for all internal blocks independently (gating clock mechanism used when no activity)

CHAPTER
THREE

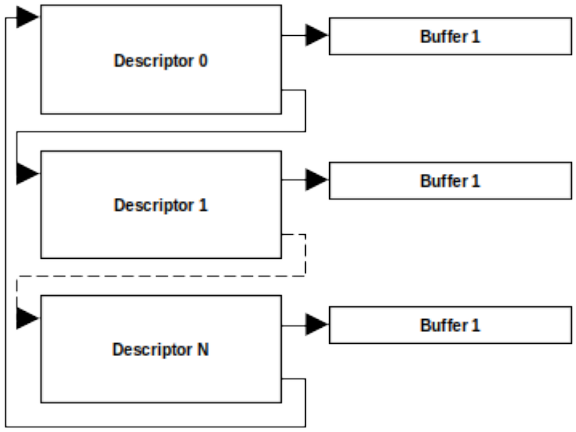
PROGRAMMING

3.1 Descriptor Lists and Data Buffers

The EMAC transfers frame data to and from receive and transmit buffers in host memory. The descriptors resides also in the host memory and acts as pointers to these buffers.
There are two descriptor lists, one for the receive buffers and one for transmit. The base address of each list is written into CSR3 and CSR4, respectively. A descriptor list is forward-linked, either implicitly or explicitly. The last descriptor may point back to the first entry to create a ring structure. Explicit chaining of descriptors is accomplished by setting the second address chained in both receive and transmit descriptors. The descriptor lists reside in the host physical memory address space. Each descriptor can point to a maximum of two buffers. This enables two buffers to be used, physically addressed, and not contiguous in memory.
A data buffer consists of either an entire frame or part of a frame, but it cannot exceed a single frame. Buffers contain only data. The buffer status is maintained in the descriptor. Data chaining refers to frames that span multiple data buffers. Data chaining can be enabled or disabled. The data buffers also reside in the host physical memory space.
Descriptor Ring Configuration:

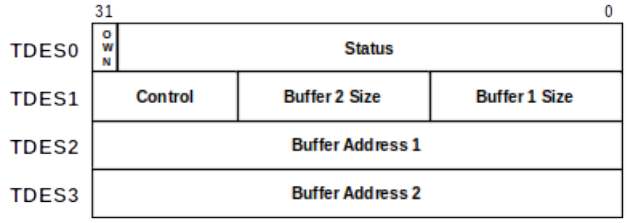


Descriptor Chain Configuration:



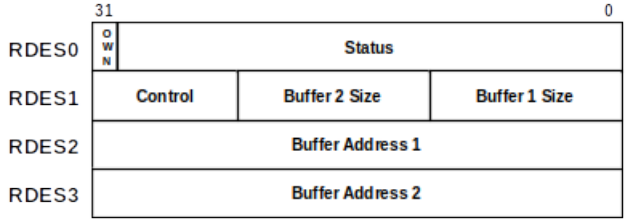
3.2 Transmit descriptors

Descriptors and receive buffer addresses must be 32-bit word aligned.
Providing two buffers, two byte-count buffers, and two address pointers in each descriptor enables the adapter port to be compatible with various types of memory management schemes.
Transmit Descriptor Format:



3.3 Receive descriptors

Descriptors and receive buffer addresses must be 32-bit word aligned.
Providing two buffers, two byte-count buffers, and two address pointers in each descriptor enables the adapter port to be compatible with various types of memory management schemes.
Receive Descriptor Format:



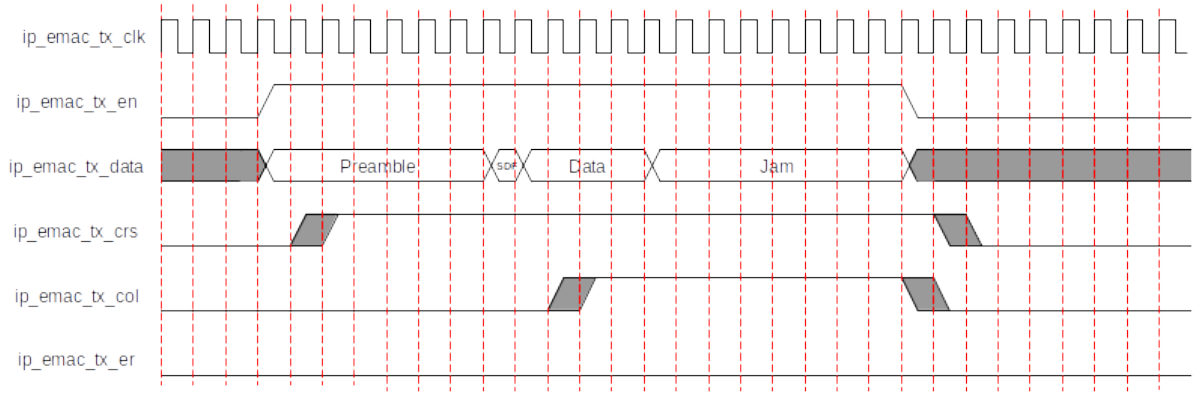
CHAPTER
FOUR

TIMING

All waveforms given in this section illustrate the behavior of the EMAC block assuming a typical IEEE 802.3-2002 behavior for the remote port.

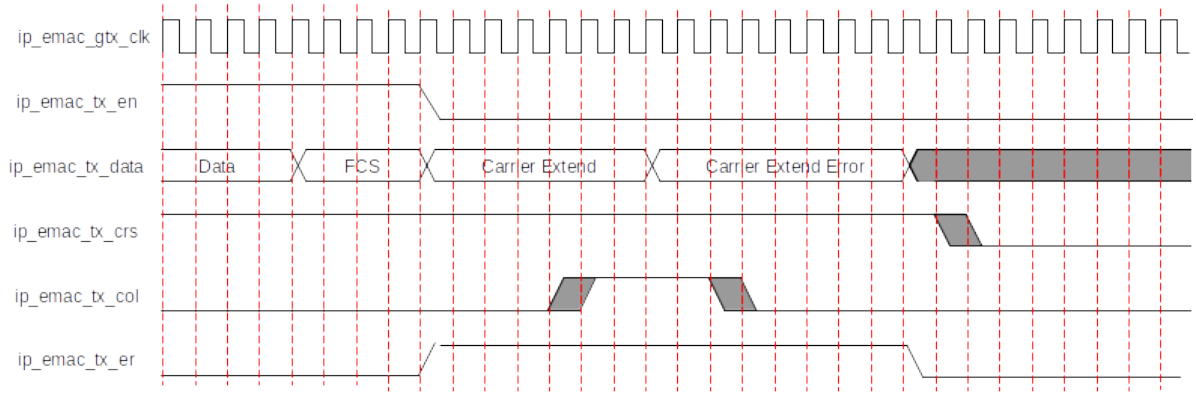
4.1 Early Collision Timing

10/100Mbps Early Collision Behavior:



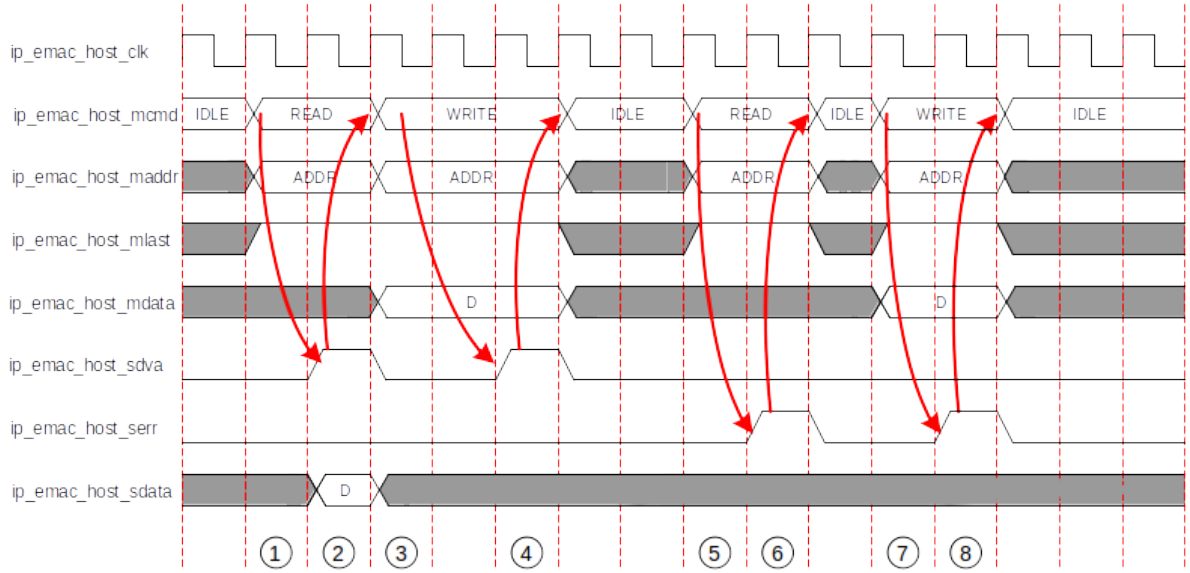
This figure describes a MII early collision behavior. The packet is retransmitted after defer and backoff period.

1000Mbps Early Collision Behavior:



This figure describes a GMII early collision behavior. The packet is retransmitted after defer and backoff period.

4.2 Host Master Interface Single Read/Write Timing



This figure presents the host interface timing when single commands are used. The *ip_emac_host_mlast* asserted high indicates that single command is issued. The *ip_emac_host_mcmd* transition to IDLE is determined by the assertion of *ip_emac_host_sdva* or *ip_emac_host_serr* signal. After the slave response for the current command the next command is loaded by the *ip_emac_host_mcmd* if available, else the IDLE state is loaded.

1. The EMAC issues a single READ command
2. The slave responds by asserting *ip_emac_host_sdva* and *ip_emac_host_sdata*
3. The EMAC issues a single WRITE command
4. The slave accepts the WRITE command by asserting *ip_emac_host_sdva*
5. The EMAC issues a single READ command
6. The slave responds by asserting *ip_emac_host_serr* (the transfer cannot be complete by the slave)
7. The EMAC issues a single WRITE command
8. The slave responds by asserting *ip_emac_host_serr* (the transfer cannot be complete by the slave)

CHAPTER
FIVE

DESIGN TOPS

5.1 Module ip_emac_top

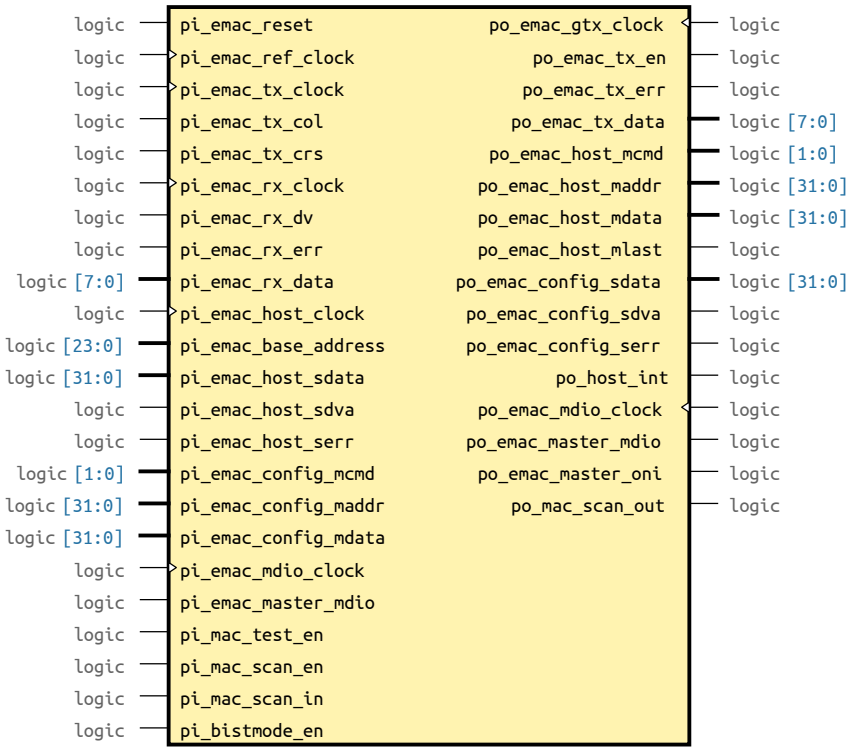


Fig. 1: Block Diagram of ip_emac_top

Table 1: Ports

Name	Type	Direction	Description
pi_emac_reset	wire logic	input	Global Hardware reset (active low)
pi_emac_ref_clock	wire logic	input	GMII 125 MHz reference clock
pi_emac_tx_clock	wire logic	input	Transmit GMII/MII interface Transmit MII 25/2.5 MHz clock (from PHY)
po_emac_gtx_clock	wire logic	output	Transmit GMII 125 MHz clock (to PHY)
po_emac_tx_en	wire logic	output	Transmit MII/GMII enable indication (to PHY)

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Table 1 – continued from previous page

Name	Type	Direction	Description
po_emac_tx_err	wire logic	output	Transmit MII/GMII error indication (to PHY)
po_emac_tx_data	wire logic [7 : 0]	output	Transmit MII/GMII data (MII data is po_-emac_tx_data[3:0]) (to PHY)
pi_emac_tx_col	wire logic	input	Collision indication (from PHY)
pi_emac_tx_crs	wire logic	input	Carrier Sense indication (from PHY)
pi_emac_rx_clock	wire logic	input	Receive GMII/MII interface Receive GMI-I/MII 125/25/2.5 MHz clock (from PHY)
pi_emac_rx_dv	wire logic	input	Receive MII/GMII data valid indication (from PHY)
pi_emac_rx_err	wire logic	input	Receive MII/GMII error indication (from PHY)
pi_emac_rx_data	wire logic [7 : 0]	input	Receive MII/GMII data (MII data is pi_-emac_rx_data[3:0]) (from PHY)
pi_emac_host_clock	wire logic	input	HOST interface (common)
pi_emac_base_address	wire logic [23 : 0]	input	host data interface
po_emac_host_mcmd	wire logic [1 : 0]	output	
po_emac_host_maddr	wire logic [31 : 0]	output	
po_emac_host_mdata	wire logic [31 : 0]	output	
po_emac_host_mlast	wire logic	output	
pi_emac_host_sdata	wire logic [31 : 0]	input	
pi_emac_host_sdva	wire logic	input	
pi_emac_host_serr	wire logic	input	
pi_emac_config_mcmd	wire logic [1 : 0]	input	host config interface
pi_emac_config_maddr	wire logic [31 : 0]	input	
pi_emac_config_mdata	wire logic [31 : 0]	input	
po_emac_config_sdata	wire logic [31 : 0]	output	pi_emac_config_mlast ,
po_emac_config_sdva	wire logic	output	
po_emac_config_serr	wire logic	output	

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Table 1 – continued from previous page

Name	Type	Direction	Description
po_host_int	wire logic	output	general interrupt to host
pi_emac_mdio_clock	wire logic	input	MDIO interface
po_emac_mdio_clock	wire logic	output	
pi_emac_master_mdio	wire logic	input	
po_emac_master_mdio	wire logic	output	
po_emac_master_oni	wire logic	output	
pi_mac_test_en	wire logic	input	Test and Scan interface signals
pi_mac_scan_en	wire logic	input	
pi_mac_scan_in	wire logic	input	
po_mac_scan_out	wire logic	output	
pi_bistmode_en	wire logic	input	

Submodules

ip_emac_top
↪host_clk_mng : *ip_host_clk_mng_g*
↪host_if : *ip_mac_hostif_top*
↪mac_top : *ip_mac_top_g* #(.TX_MEM_ADDR(10), .RX_MEM_ADDR(10))
↪regs_bank : *ip_mac_regs_bank*

CHAPTER
SIX

MODULES

6.1 Module cts_buffer

Fig. 1: Block Diagram of cts_buffer

Table 1: Ports

Name	Type	Direction	Description
cts_buff_in	wire logic	input	a CTS buffer input clock
cts_buff_out	wire logic	output	a CTS buffer output clock

Instances

ip_emac_top : *ip_emac_top*
↪host_clk_mng : *ip_host_clk_mng_g*
↪host_free_clock : *ip_gate_clock_g*
↪output_cts : *cts_buffer*
↪host_gate_clock_1 : *ip_gate_clock_g*
↪output_cts : *cts_buffer*
↪host_gate_clock_2 : *ip_gate_clock_g*
↪output_cts : *cts_buffer*
↪host_gate_clock_3 : *ip_gate_clock_g*
↪output_cts : *cts_buffer*
↪host_gate_clock_4 : *ip_gate_clock_g*
↪output_cts : *cts_buffer*
↪host_gate_clock_5 : *ip_gate_clock_g*
↪output_cts : *cts_buffer*
↪mac_top : *ip_mac_top_g*
↪mac_clk_mng : *ip_mac_clk_mng_g*
↪gtx_clock_out : *ip_gate_clock_g*
↪output_cts : *cts_buffer*
↪host_free_clock : *ip_gate_clock_g*
↪output_cts : *cts_buffer*
↪host_gate_clock_1 : *ip_gate_clock_g*
↪output_cts : *cts_buffer*
↪mdio_free_clock : *ip_gate_clock_g*
↪output_cts : *cts_buffer*
↪rx_free_clock : *ip_gate_clock_g*
↪output_cts : *cts_buffer*
↪rx_gate_clock_1 : *ip_gate_clock_g*
↪output_cts : *cts_buffer*

↪rx_gate_clock_2 : *ip_gate_clock_g*
↪output_cts : *cts_buffer*
↪rx_gate_clock_3 : *ip_gate_clock_g*
↪output_cts : *cts_buffer*
↪tx_free_clock : *ip_gate_clock_g*
↪output_cts : *cts_buffer*
↪tx_gate_clock_1 : *ip_gate_clock_g*
↪output_cts : *cts_buffer*
↪tx_gate_clock_2 : *ip_gate_clock_g*
↪output_cts : *cts_buffer*
↪tx_gate_clock_3 : *ip_gate_clock_g*
↪output_cts : *cts_buffer*
↪tx_gate_clock_4 : *ip_gate_clock_g*
↪output_cts : *cts_buffer*

6.2 Module dff_metastable

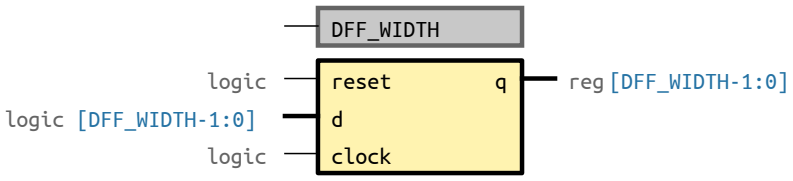

Fig. 2: Block Diagram of dff_metastable

Table 2: Parameters

Name	Default	Description
DFF_WIDTH	1	

Table 3: Ports

Name	Type	Direction	Description
reset	wire logic	input	
d	wire logic [*DFF_WIDTH* - 1 : 0]	input	
clock	wire logic	input	
q	reg [*DFF_WIDTH* - 1 : 0]	output	

Always Blocks

`always@(i_q)`

Simulation model (metastability)

Instances

ip_emac_top : *ip_emac_top*
↪mac_top : *ip_mac_top_g*
↪mac_rx_top : *ip_mac_rx_top_g*
↪rx_async : *ip_async_fifo_g*
↪cell_0 : *ip_sync_cell*
↪metastable_toggle_rd : *dff_metastable* #(.DFF_WIDTH(1))
↪metastable_toggle_wr : *dff_metastable* #(.DFF_WIDTH(1))
↪cell_1 : *ip_sync_cell*
↪metastable_toggle_rd : *dff_metastable* #(.DFF_WIDTH(1))
↪metastable_toggle_wr : *dff_metastable* #(.DFF_WIDTH(1))
↪cell_2 : *ip_sync_cell*
↪metastable_toggle_rd : *dff_metastable* #(.DFF_WIDTH(1))
↪metastable_toggle_wr : *dff_metastable* #(.DFF_WIDTH(1))
↪cell_3 : *ip_sync_cell*
↪metastable_toggle_rd : *dff_metastable* #(.DFF_WIDTH(1))
↪metastable_toggle_wr : *dff_metastable* #(.DFF_WIDTH(1))
↪cell_4 : *ip_sync_cell*
↪metastable_toggle_rd : *dff_metastable* #(.DFF_WIDTH(1))

↪metastable_toggle_wr : *dff_metastable* #(.DFF_WIDTH(1))
↪cell_5 : *ip_sync_cell*
↪metastable_toggle_rd : *dff_metastable* #(.DFF_WIDTH(1))
↪metastable_toggle_wr : *dff_metastable* #(.DFF_WIDTH(1))
↪cell_6 : *ip_sync_cell*
↪metastable_toggle_rd : *dff_metastable* #(.DFF_WIDTH(1))
↪metastable_toggle_wr : *dff_metastable* #(.DFF_WIDTH(1))
↪cell_7 : *ip_sync_cell*
↪metastable_toggle_rd : *dff_metastable* #(.DFF_WIDTH(1))
↪metastable_toggle_wr : *dff_metastable* #(.DFF_WIDTH(1))
↪mac_tx_top : *ip_mac_tx_top_g*
↪tx_data_async : *ip_async_fifo_g*
↪cell_0 : *ip_sync_cell*
↪metastable_toggle_rd : *dff_metastable* #(.DFF_WIDTH(1))
↪metastable_toggle_wr : *dff_metastable* #(.DFF_WIDTH(1))
↪cell_1 : *ip_sync_cell*
↪metastable_toggle_rd : *dff_metastable* #(.DFF_WIDTH(1))
↪metastable_toggle_wr : *dff_metastable* #(.DFF_WIDTH(1))
↪cell_2 : *ip_sync_cell*
↪metastable_toggle_rd : *dff_metastable* #(.DFF_WIDTH(1))
↪metastable_toggle_wr : *dff_metastable* #(.DFF_WIDTH(1))
↪cell_3 : *ip_sync_cell*
↪metastable_toggle_rd : *dff_metastable* #(.DFF_WIDTH(1))
↪metastable_toggle_wr : *dff_metastable* #(.DFF_WIDTH(1))
↪cell_4 : *ip_sync_cell*
↪metastable_toggle_rd : *dff_metastable* #(.DFF_WIDTH(1))
↪metastable_toggle_wr : *dff_metastable* #(.DFF_WIDTH(1))
↪cell_5 : *ip_sync_cell*
↪metastable_toggle_rd : *dff_metastable* #(.DFF_WIDTH(1))
↪metastable_toggle_wr : *dff_metastable* #(.DFF_WIDTH(1))
↪cell_6 : *ip_sync_cell*
↪metastable_toggle_rd : *dff_metastable* #(.DFF_WIDTH(1))
↪metastable_toggle_wr : *dff_metastable* #(.DFF_WIDTH(1))
↪cell_7 : *ip_sync_cell*
↪metastable_toggle_rd : *dff_metastable* #(.DFF_WIDTH(1))
↪metastable_toggle_wr : *dff_metastable* #(.DFF_WIDTH(1))
↪tx_stat_async : *ip_async_fifo_g*
↪cell_0 : *ip_sync_cell*
↪metastable_toggle_rd : *dff_metastable* #(.DFF_WIDTH(1))
↪metastable_toggle_wr : *dff_metastable* #(.DFF_WIDTH(1))
↪cell_1 : *ip_sync_cell*
↪metastable_toggle_rd : *dff_metastable* #(.DFF_WIDTH(1))
↪metastable_toggle_wr : *dff_metastable* #(.DFF_WIDTH(1))
↪cell_2 : *ip_sync_cell*
↪metastable_toggle_rd : *dff_metastable* #(.DFF_WIDTH(1))
↪metastable_toggle_wr : *dff_metastable* #(.DFF_WIDTH(1))
↪cell_3 : *ip_sync_cell*
↪metastable_toggle_rd : *dff_metastable* #(.DFF_WIDTH(1))
↪metastable_toggle_wr : *dff_metastable* #(.DFF_WIDTH(1))
↪cell_4 : *ip_sync_cell*
↪metastable_toggle_rd : *dff_metastable* #(.DFF_WIDTH(1))
↪metastable_toggle_wr : *dff_metastable* #(.DFF_WIDTH(1))
↪cell_5 : *ip_sync_cell*
↪metastable_toggle_rd : *dff_metastable* #(.DFF_WIDTH(1))
↪metastable_toggle_wr : *dff_metastable* #(.DFF_WIDTH(1))
↪cell_6 : *ip_sync_cell*
↪metastable_toggle_rd : *dff_metastable* #(.DFF_WIDTH(1))
↪metastable_toggle_wr : *dff_metastable* #(.DFF_WIDTH(1))

↪cell_7 : *ip_sync_cell*
↪metastable_toggle_rd : *dff_metastable* #(.DFF_WIDTH(1))
↪metastable_toggle_wr : *dff_metastable* #(.DFF_WIDTH(1))

Submodules

dff_metastable #(.DFF_WIDTH(1))
↪dffrhqx1_0 : *dffrhqx1*

6.3 Module dffrhqx1

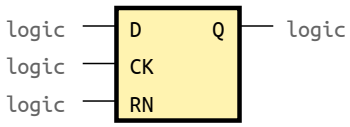

Fig. 3: Block Diagram of dffrhqx1

Table 4: Ports

Name	Type	Direction	Description
Q	wire logic	output	
D	wire logic	input	
CK	wire logic	input	
RN	wire logic	input	

Instances

ip_emac_top : *ip_emac_top*
↪mac_top : *ip_mac_top_g*
↪mac_rx_top : *ip_mac_rx_top_g*
↪rx_async : *ip_async_fifo_g*
↪cell_0 : *ip_sync_cell*
↪metastable_toggle_rd : *dff_metastable*
↪dffrhqx1_0 : *dffrhqx1*
↪metastable_toggle_wr : *dff_metastable*
↪dffrhqx1_0 : *dffrhqx1*
↪cell_1 : *ip_sync_cell*
↪metastable_toggle_rd : *dff_metastable*
↪dffrhqx1_0 : *dffrhqx1*
↪metastable_toggle_wr : *dff_metastable*
↪dffrhqx1_0 : *dffrhqx1*
↪cell_2 : *ip_sync_cell*
↪metastable_toggle_rd : *dff_metastable*
↪dffrhqx1_0 : *dffrhqx1*
↪metastable_toggle_wr : *dff_metastable*
↪dffrhqx1_0 : *dffrhqx1*
↪cell_3 : *ip_sync_cell*
↪metastable_toggle_rd : *dff_metastable*
↪dffrhqx1_0 : *dffrhqx1*
↪metastable_toggle_wr : *dff_metastable*
↪dffrhqx1_0 : *dffrhqx1*
↪cell_4 : *ip_sync_cell*
↪metastable_toggle_rd : *dff_metastable*
↪dffrhqx1_0 : *dffrhqx1*
↪metastable_toggle_wr : *dff_metastable*
↪dffrhqx1_0 : *dffrhqx1*
↪cell_5 : *ip_sync_cell*
↪metastable_toggle_rd : *dff_metastable*
↪dffrhqx1_0 : *dffrhqx1*

↪metastable_toggle_wr : *dff_metastable*
↪dffrhqx1_0 : *dffrhqx1*
↪cell_6 : *ip_sync_cell*
↪metastable_toggle_rd : *dff_metastable*
↪dffrhqx1_0 : *dffrhqx1*
↪metastable_toggle_wr : *dff_metastable*
↪dffrhqx1_0 : *dffrhqx1*
↪cell_7 : *ip_sync_cell*
↪metastable_toggle_rd : *dff_metastable*
↪dffrhqx1_0 : *dffrhqx1*
↪metastable_toggle_wr : *dff_metastable*
↪dffrhqx1_0 : *dffrhqx1*
↪mac_tx_top : *ip_mac_tx_top_g*
↪tx_data_async : *ip_async_fifo_g*
↪cell_0 : *ip_sync_cell*
↪metastable_toggle_rd : *dff_metastable*
↪dffrhqx1_0 : *dffrhqx1*
↪metastable_toggle_wr : *dff_metastable*
↪dffrhqx1_0 : *dffrhqx1*
↪cell_1 : *ip_sync_cell*
↪metastable_toggle_rd : *dff_metastable*
↪dffrhqx1_0 : *dffrhqx1*
↪metastable_toggle_wr : *dff_metastable*
↪dffrhqx1_0 : *dffrhqx1*
↪cell_2 : *ip_sync_cell*
↪metastable_toggle_rd : *dff_metastable*
↪dffrhqx1_0 : *dffrhqx1*
↪metastable_toggle_wr : *dff_metastable*
↪dffrhqx1_0 : *dffrhqx1*
↪cell_3 : *ip_sync_cell*
↪metastable_toggle_rd : *dff_metastable*
↪dffrhqx1_0 : *dffrhqx1*
↪metastable_toggle_wr : *dff_metastable*
↪dffrhqx1_0 : *dffrhqx1*
↪cell_4 : *ip_sync_cell*
↪metastable_toggle_rd : *dff_metastable*
↪dffrhqx1_0 : *dffrhqx1*
↪metastable_toggle_wr : *dff_metastable*
↪dffrhqx1_0 : *dffrhqx1*
↪cell_5 : *ip_sync_cell*
↪metastable_toggle_rd : *dff_metastable*
↪dffrhqx1_0 : *dffrhqx1*
↪metastable_toggle_wr : *dff_metastable*
↪dffrhqx1_0 : *dffrhqx1*
↪cell_6 : *ip_sync_cell*
↪metastable_toggle_rd : *dff_metastable*
↪dffrhqx1_0 : *dffrhqx1*
↪metastable_toggle_wr : *dff_metastable*
↪dffrhqx1_0 : *dffrhqx1*
↪cell_7 : *ip_sync_cell*
↪metastable_toggle_rd : *dff_metastable*
↪dffrhqx1_0 : *dffrhqx1*
↪metastable_toggle_wr : *dff_metastable*
↪dffrhqx1_0 : *dffrhqx1*
↪tx_stat_async : *ip_async_fifo_g*
↪cell_0 : *ip_sync_cell*
↪metastable_toggle_rd : *dff_metastable*
↪dffrhqx1_0 : *dffrhqx1*

↪metastable_toggle_wr : *dff_metastable*
↪dffrhqx1_0 : *dffrhqx1*
↪cell_1 : *ip_sync_cell*
↪metastable_toggle_rd : *dff_metastable*
↪dffrhqx1_0 : *dffrhqx1*
↪metastable_toggle_wr : *dff_metastable*
↪dffrhqx1_0 : *dffrhqx1*
↪cell_2 : *ip_sync_cell*
↪metastable_toggle_rd : *dff_metastable*
↪dffrhqx1_0 : *dffrhqx1*
↪metastable_toggle_wr : *dff_metastable*
↪dffrhqx1_0 : *dffrhqx1*
↪cell_3 : *ip_sync_cell*
↪metastable_toggle_rd : *dff_metastable*
↪dffrhqx1_0 : *dffrhqx1*
↪metastable_toggle_wr : *dff_metastable*
↪dffrhqx1_0 : *dffrhqx1*
↪cell_4 : *ip_sync_cell*
↪metastable_toggle_rd : *dff_metastable*
↪dffrhqx1_0 : *dffrhqx1*
↪metastable_toggle_wr : *dff_metastable*
↪dffrhqx1_0 : *dffrhqx1*
↪cell_5 : *ip_sync_cell*
↪metastable_toggle_rd : *dff_metastable*
↪dffrhqx1_0 : *dffrhqx1*
↪metastable_toggle_wr : *dff_metastable*
↪dffrhqx1_0 : *dffrhqx1*
↪cell_6 : *ip_sync_cell*
↪metastable_toggle_rd : *dff_metastable*
↪dffrhqx1_0 : *dffrhqx1*
↪metastable_toggle_wr : *dff_metastable*
↪dffrhqx1_0 : *dffrhqx1*
↪cell_7 : *ip_sync_cell*
↪metastable_toggle_rd : *dff_metastable*
↪dffrhqx1_0 : *dffrhqx1*
↪metastable_toggle_wr : *dff_metastable*
↪dffrhqx1_0 : *dffrhqx1*

6.4 Module dram_001

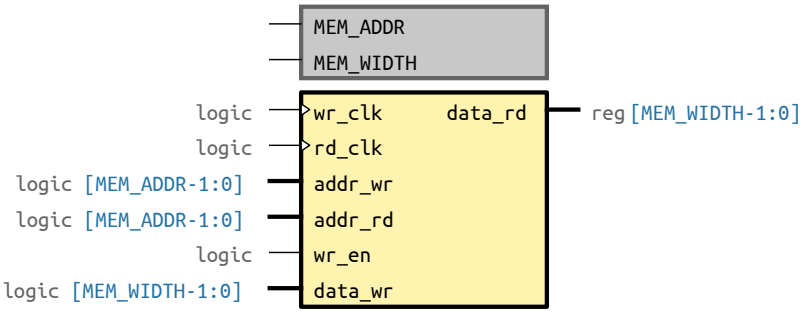

Fig. 4: Block Diagram of dram_001

Table 5: Parameters

Name	Default	Description
MEM_ADDR	5	Address width (9 -> 512 locations, 10->1024)
MEM_WIDTH	16	Data width

Table 6: Ports

Name	Type	Direction	Description
wr_clk	wire logic	input	Write clock
rd_clk	wire logic	input	Read clock
addr_wr	wire logic [*MEM_ADDR* - 1 : 0]	input	Write address
addr_rd	wire logic [*MEM_ADDR* - 1 : 0]	input	Read address
wr_en	wire logic	input	Write enable
data_wr	wire logic [*MEM_WIDTH* - 1 : 0]	input	Write data
data_rd	reg [*MEM_WIDTH* - 1 : 0]	output	Read data (registered)

Always Blocks

`always@(posedge wr_clk)`

Memory Write

`always@(posedge rd_clk)`

Memory Read

Instances

ip_emac_top : *ip_emac_top*
↪mac_top : *ip_mac_top_g*
↪mac_rx_top : *ip_mac_rx_top_g*
↪rx_data_dram : *ip_mac_dram_002*

```
            ↪dram_001 : dram_001 #(.MEM_ADDR(10), .MEM_WIDTH(37))
        ↪rx_dram_hash_0 : ip_mac_dram_004
            ↪dram_001 : dram_001 #(.MEM_ADDR(4), .MEM_WIDTH(32))
        ↪rx_dram_hash_1 : ip_mac_dram_003
            ↪dram_001 : dram_001 #(.MEM_ADDR(4), .MEM_WIDTH(16))
↪mac_tx_top : ip_mac_tx_top_g
        ↪tx_data_dram : ip_mac_dram_001
            ↪dram_001 : dram_001 #(.MEM_ADDR(10), .MEM_WIDTH(39))
```

6.5 Module gate_clock_cell_g

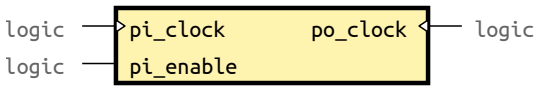

Fig. 5: Block Diagram of gate_clock_cell_g

Table 7: Ports

Name	Type	Direction	Description
pi_clock	wire logic	input	Input functional clock
po_clock	wire logic	output	Output gated clock (multiplexed with test clock)
pi_enable	wire logic	input	Enable output clock

Always Blocks

always@(pi_clock)

Low Level Transparent Latch Process

Instances

ip_emac_top : *ip_emac_top*
- ↪host_clk_mng : *ip_host_clk_mng_g*
  - ↪host_free_clock : *ip_gate_clock_g*
    - ↪gate_clock : *gate_clock_cell_g*
  - ↪host_gate_clock_1 : *ip_gate_clock_g*
    - ↪gate_clock : *gate_clock_cell_g*
  - ↪host_gate_clock_2 : *ip_gate_clock_g*
    - ↪gate_clock : *gate_clock_cell_g*
  - ↪host_gate_clock_3 : *ip_gate_clock_g*
    - ↪gate_clock : *gate_clock_cell_g*
  - ↪host_gate_clock_4 : *ip_gate_clock_g*
    - ↪gate_clock : *gate_clock_cell_g*
  - ↪host_gate_clock_5 : *ip_gate_clock_g*
    - ↪gate_clock : *gate_clock_cell_g*
- ↪mac_top : *ip_mac_top_g*
  - ↪mac_clk_mng : *ip_mac_clk_mng_g*
    - ↪gtx_clock_out : *ip_gate_clock_g*
      - ↪gate_clock : *gate_clock_cell_g*
    - ↪host_free_clock : *ip_gate_clock_g*
      - ↪gate_clock : *gate_clock_cell_g*
    - ↪host_gate_clock_1 : *ip_gate_clock_g*
      - ↪gate_clock : *gate_clock_cell_g*
    - ↪mdio_free_clock : *ip_gate_clock_g*
      - ↪gate_clock : *gate_clock_cell_g*
    - ↪rx_free_clock : *ip_gate_clock_g*
      - ↪gate_clock : *gate_clock_cell_g*
    - ↪rx_gate_clock_1 : *ip_gate_clock_g*
      - ↪gate_clock : *gate_clock_cell_g*
    - ↪rx_gate_clock_2 : *ip_gate_clock_g*

↪gate_clock : *gate_clock_cell_g*
↪rx_gate_clock_3 : *ip_gate_clock_g*
↪gate_clock : *gate_clock_cell_g*
↪tx_free_clock : *ip_gate_clock_g*
↪gate_clock : *gate_clock_cell_g*
↪tx_gate_clock_1 : *ip_gate_clock_g*
↪gate_clock : *gate_clock_cell_g*
↪tx_gate_clock_2 : *ip_gate_clock_g*
↪gate_clock : *gate_clock_cell_g*
↪tx_gate_clock_3 : *ip_gate_clock_g*
↪gate_clock : *gate_clock_cell_g*
↪tx_gate_clock_4 : *ip_gate_clock_g*
↪gate_clock : *gate_clock_cell_g*

6.6 Module ip_async_fifo_g

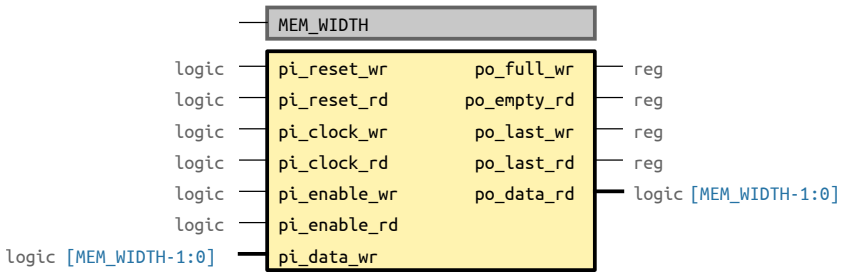

Fig. 6: Block Diagram of ip_async_fifo_g

Overview

Asynchronous FIFOs are used in designs to safely pass multi-bit data words from one clock domain to another.

Data words are placed into a FIFO buffer memory array by: - control signals in one clock domain - and the data words are removed from another port of the same FIFO buffer memory array by control signals from a second clock domain.

Table 8: Parameters

Name	Default	Description
MEM_WIDTH	32	Data width

Table 9: Ports

Name	Type	Direction	Description
pi_reset_wr	wire logic	input	Write synchronous reset
pi_reset_rd	wire logic	input	Read synchronous reset
pi_clock_wr	wire logic	input	Write clock
pi_clock_rd	wire logic	input	Read clock
pi_enable_wr	wire logic	input	Write enable
pi_enable_rd	wire logic	input	Read enable
po_full_wr	reg	output	FIFO full indication
po_empty_rd	reg	output	FIFO empty indication
po_last_wr	reg	output	FIFO last location for write (almoast full)
po_last_rd	reg	output	FIFO last location for read (almoast empty)
pi_data_wr	wire logic [*MEM_WIDTH* - 1 : 0]	input	FIFO data input

continues on next page

Table 9 – continued from previous page

Name	Type	Direction	Description
po_data_rd	wire logic [*MEM_WIDTH* - 1 : 0]	output	FIFO data output

Always Blocks

always@(posedge pi_clock_wr)

Data Path - Input Selection Process

always@(ring_wr or pi_enable_wr)

Assert ready write signal according with the write address value

always@(posedge pi_clock_wr or negedge pi_reset_wr)

Write Pointer Updated when Write Access is performed

always@(ring_rd or pi_enable_rd)

assert ready read signal according with the read address value

always@(posedge pi_clock_rd or negedge pi_reset_rd)

Read Pointer Updated when Read Access is performed *

Instances

ip_emac_top : *ip_emac_top*
↪mac_top : *ip_mac_top_g*
↪mac_rx_top : *ip_mac_rx_top_g*
↪rx_async : *ip_async_fifo_g* #(.MEM_WIDTH(37))
↪mac_tx_top : *ip_mac_tx_top_g*
↪tx_data_async : *ip_async_fifo_g* #(.MEM_WIDTH(39))
↪tx_stat_async : *ip_async_fifo_g* #(.MEM_WIDTH(10))

Submodules

ip_async_fifo_g #(.MEM_WIDTH(37))
↪cell_0 : *ip_sync_cell*
↪cell_1 : *ip_sync_cell*
↪cell_2 : *ip_sync_cell*
↪cell_3 : *ip_sync_cell*
↪cell_4 : *ip_sync_cell*
↪cell_5 : *ip_sync_cell*
↪cell_6 : *ip_sync_cell*
↪cell_7 : *ip_sync_cell*
ip_async_fifo_g #(.MEM_WIDTH(39))
↪cell_0 : *ip_sync_cell*
↪cell_1 : *ip_sync_cell*
↪cell_2 : *ip_sync_cell*
↪cell_3 : *ip_sync_cell*
↪cell_4 : *ip_sync_cell*
↪cell_5 : *ip_sync_cell*
↪cell_6 : *ip_sync_cell*
↪cell_7 : *ip_sync_cell*
ip_async_fifo_g #(.MEM_WIDTH(10))
↪cell_0 : *ip_sync_cell*
↪cell_1 : *ip_sync_cell*
↪cell_2 : *ip_sync_cell*
↪cell_3 : *ip_sync_cell*
↪cell_4 : *ip_sync_cell*
↪cell_5 : *ip_sync_cell*
↪cell_6 : *ip_sync_cell*
↪cell_7 : *ip_sync_cell*

6.7 Module ip_gate_clock_g

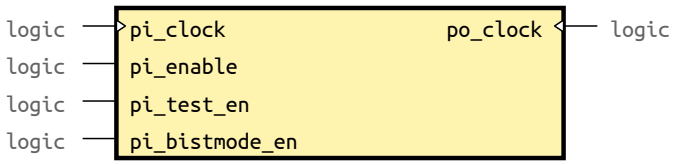

Fig. 7: Block Diagram of ip_gate_clock_g

Table 10: Ports

Name	Type	Direction	Description
pi_clock	wire logic	input	Input free running clock
pi_enable	wire logic	input	Enable output clock
pi_test_en	wire logic	input	Test enable
pi_bistmode_en	wire logic	input	
po_clock	wire logic	output	Output free running clock

Instances

ip_emac_top : *ip_emac_top*
- ↪host_clk_mng : *ip_host_clk_mng_g*
  - ↪host_free_clock : *ip_gate_clock_g*
  - ↪host_gate_clock_1 : *ip_gate_clock_g*
  - ↪host_gate_clock_2 : *ip_gate_clock_g*
  - ↪host_gate_clock_3 : *ip_gate_clock_g*
  - ↪host_gate_clock_4 : *ip_gate_clock_g*
  - ↪host_gate_clock_5 : *ip_gate_clock_g*
- ↪mac_top : *ip_mac_top_g*
  - ↪mac_clk_mng : *ip_mac_clk_mng_g*
    - ↪gtx_clock_out : *ip_gate_clock_g*
    - ↪host_free_clock : *ip_gate_clock_g*
    - ↪host_gate_clock_1 : *ip_gate_clock_g*
    - ↪mdio_free_clock : *ip_gate_clock_g*
    - ↪rx_free_clock : *ip_gate_clock_g*
    - ↪rx_gate_clock_1 : *ip_gate_clock_g*
    - ↪rx_gate_clock_2 : *ip_gate_clock_g*
    - ↪rx_gate_clock_3 : *ip_gate_clock_g*
    - ↪tx_free_clock : *ip_gate_clock_g*
    - ↪tx_gate_clock_1 : *ip_gate_clock_g*
    - ↪tx_gate_clock_2 : *ip_gate_clock_g*
    - ↪tx_gate_clock_3 : *ip_gate_clock_g*
    - ↪tx_gate_clock_4 : *ip_gate_clock_g*

Submodules

ip_gate_clock_g
  ↪gate_clock : *gate_clock_cell_g*
  ↪output_cts : *cts_buffer*

6.8 Module ip_host_clk_mng_g

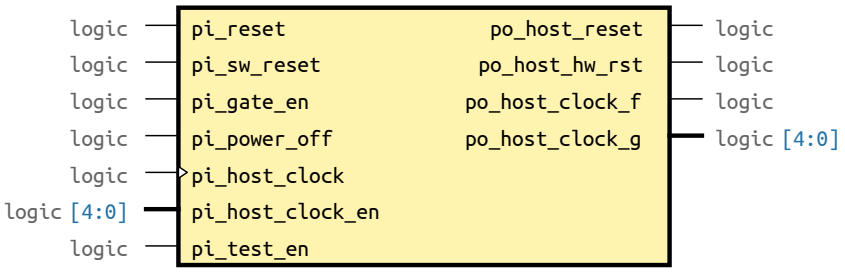

Fig. 8: Block Diagram of ip_host_clk_mng_g

Table 11: Ports

Name	Type	Direction	Description
pi_reset	wire logic	input	Resets Hardware reset (active low)
pi_sw_reset	wire logic	input	Software reset (active high)
pi_gate_en	wire logic	input	Auto Gating Clock Enable (power saving)
po_host_reset	wire logic	output	Hardware/Software Global output reset (HOST clock domain)
po_host_hw_rst	wire logic	output	Hardware Global output reset (HOST clock domain)
pi_power_off	wire logic	input	Power OFF Power off (all internal clocks are disabled)
pi_host_clock	wire logic	input	Clocks HOST clock used by the reset synchronization block
pi_host_clock_en	wire logic [4 : 0]	input	HOST clock enable
po_host_clock_f	wire logic	output	Output Host Clock Host Free Clock
po_host_clock_g	wire logic [4 : 0]	output	Host Gated Clock
pi_test_en	wire logic	input	Test and Scan interface signals Test enable (test clock select)

Instances

ip_emac_top : *ip_emac_top*
↪host_clk_mng : *ip_host_clk_mng_g*

Submodules

ip_host_clk_mng_g
↪host_free_clock : *ip_gate_clock_g*
↪host_gate_clock_1 : *ip_gate_clock_g*
↪host_gate_clock_2 : *ip_gate_clock_g*

↪host_gate_clock_3 : *ip_gate_clock_g*
↪host_gate_clock_4 : *ip_gate_clock_g*
↪host_gate_clock_5 : *ip_gate_clock_g*
↪host_sreset : *ip_sync_reset_g*
↪hw_host_sreset : *ip_sync_reset_g*

6.9 Module ip_mac_big_endian

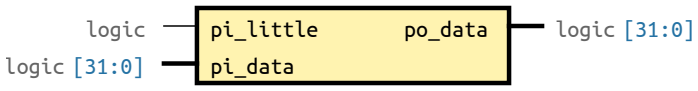

Fig. 9: Block Diagram of ip_mac_big_endian

Overview

Data should be translated to little *endian format*. The following module is a combinatorial module and is responsible to translate **a 32-bit wide data bus** (4-byte word) big endian format into a little endian organized word. When the input data is *little endian* organized the data is passed trough this block and remain unchanged.

Table 12: Ports

Name	Type	Direction	Description
pi_little	wire logic	input	Configuration Little endian
pi_data	wire logic [31 : 0]	input	Input little/big endian 32-bit word Input 32-bit data
po_data	wire logic [31 : 0]	output	Output little endian 32-bit word Output 32-bit translated data

Instances

ip_emac_top : *ip_emac_top*
↪mac_top : *ip_mac_top_g*
↪mac_rx_top : *ip_mac_rx_top_g*
↪rx_endian : *ip_mac_big_endian*
↪mac_tx_top : *ip_mac_tx_top_g*
↪tx_endian : *ip_mac_big_endian*

6.10 Module ip_mac_cfg_hash_g

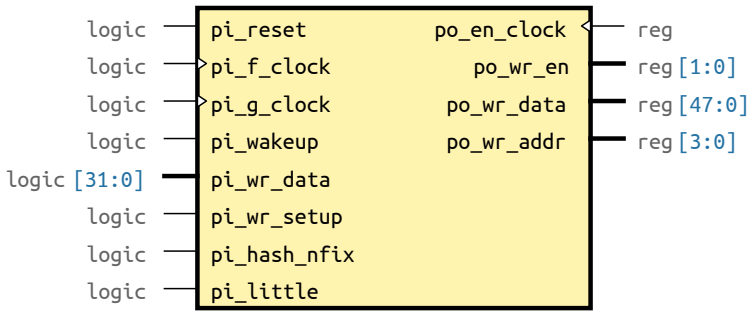

Fig. 10: Block Diagram of ip_mac_cfg_hash_g

Overview

A special configuration sequence must be performed before the reception process is started, except when it operates in promiscuous filtering mode. This is done by successively writing to CRFT configuration register. Depending on the selected filtering mode (CSR6[5:4] Filtering status field), the appropriate information should be written into the CRFT (see ***EMAC Functional Specification 1.1***)

When hash multicast or hash filtering operating mode is selected, 16 consecutive writes should be performed to the CRFT register, representing the 512-bit hash table information. After completing the hash table write, two additional writes should be performed on CRFT encapsulating the perfect 48-bit MAC address used for exact physical destination address match processing.

When perfect filtering mode is selected 32 consecutive writes should be performed to the CRFT register encapsulating 16 exact match addresses.

The structure of each 32 bit word written to CRFT register depends on CSR0[7] ***(Big/Little Endian field)*** and CSR6[5:4] (Filtering status field). See 9.2.1 and 9.2.2 for a detailed description of CRFT configuration sequence.

Table 13: Ports

Name	Type	Direction	Description
pi_reset	wire logic	input	Global Hardware Reset (host clock domain)
pi_f_clock	wire logic	input	Free HOST interface clock signal
pi_g_clock	wire logic	input	Gated HOST interface clock signal
po_en_clock	reg	output	Enable HOST interface clock signal
pi_wakeup	wire logic	input	From/To Receive DMA Wake-up internal clock used by the Setup Frame FSM,
pi_wr_data	wire logic [31 : 0]	input	should be asserted at least 2 clock cycles (HOST clock) before asserting the pi_host_wr_setup (write enable) and can be de-asserted 2 clock cycles after Setup Frame complete Setup Frame data (HOST clock synchronous)

continues on next page

Table 13 – continued from previous page

Name	Type	Direction	Description
pi_wr_setup	wire logic	input	Setup Frame write enable (HOST clock synchronous)
pi_hash_nfix	wire logic	input	Configuration Hash filtering + 1 Address match / 16 Address match
pi_little	wire logic	input	Little endian
po_wr_en	reg [1 : 0]	output	Hash Table Memory access Hash table write enable
po_wr_data	reg [47 : 0]	output	Hash table write data
po_wr_addr	reg [3 : 0]	output	Hash table write address

Always Blocks

`always@(posedge pi_g_clock or negedge pi_reset)`

FC Data Out Process

`always@(posedge pi_f_clock or negedge pi_reset)`

Gated Clock Enable

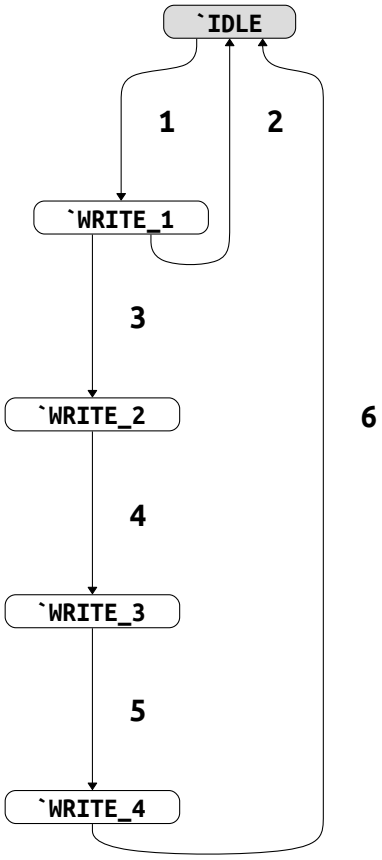

Table 14: FSM Transitions for fsm_hash_st

#	Current State	Next State	Condition	Comment
1	`IDLE	`WRITE_1	[(!(~ pi_reset) && (pi_wr_setup == 1'b1 && pi_hash_nfix == 1'b0)), (!(~ pi_reset) && !(pi_wr_setup == 1'b1 && pi_hash_nfix == 1'b0) && (pi_wr_setup == 1'b1 && pi_hash_nfix == 1'b1))]	
2	`WRITE_1	`IDLE	[(!(~ pi_reset) && (pi_wr_setup == 1'b1 && pi_hash_nfix == 1'b0))]	
3	`WRITE_1	`WRITE_2	[(!(~ pi_reset) && !(pi_wr_setup == 1'b1 && pi_hash_nfix == 1'b0) && (pi_wr_setup == 1'b1 && pi_hash_nfix == 1'b1) && (po_wr_addr == 4'hf))]	
4	`WRITE_2	`WRITE_3	[(!(~ pi_reset) && (pi_wr_setup == 1'b1))]	
5	`WRITE_3	`WRITE_4	[(!(~ pi_reset) && (pi_wr_setup == 1'b1))]	
6	`WRITE_4	`IDLE	[!(~ pi_reset)]	

Instances

ip_emac_top : *ip_emac_top*
↪mac_top : *ip_mac_top_g*
↪mac_rx_top : *ip_mac_rx_top_g*
↪cfg_hash : *ip_mac_cfg_hash_g*

6.11 Module ip_mac_clk_mng_g

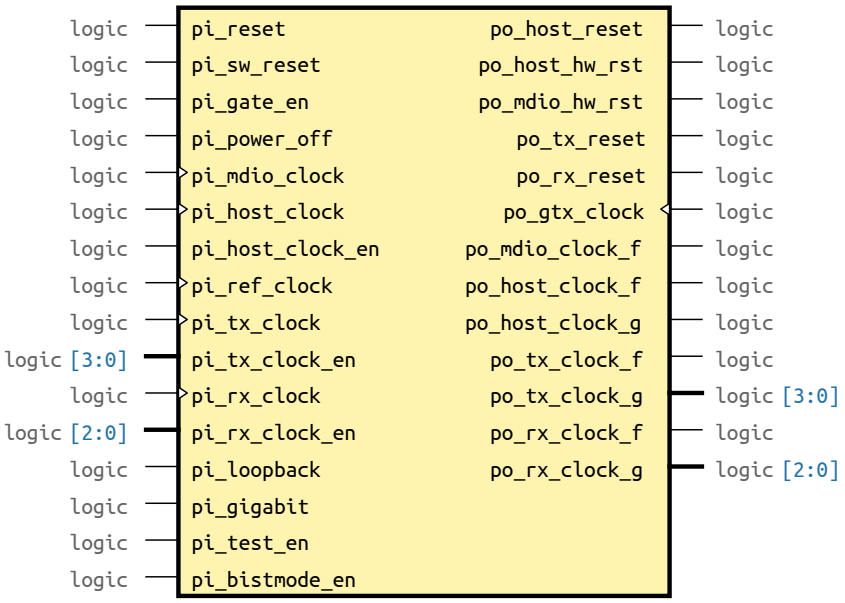

Fig. 11: Block Diagram of ip_mac_clk_mng_g

Table 15: Ports

Name	Type	Direction	Description
pi_reset	wire logic	input	Resets Hardware reset (active low)
pi_sw_reset	wire logic	input	Software reset (active high)
pi_gate_en	wire logic	input	Auto Gating Clock Enable (power saving)
po_host_reset	wire logic	output	Hardware/Software Global output reset (HOST clock domain)
po_host_hw_rst	wire logic	output	Hardware Global output reset (HOST clock domain)
po_mdio_hw_rst	wire logic	output	Hardware MDIO output reset (MDIO clock domain)
po_tx_reset	wire logic	output	Hardware/Software Global output reset (transmit clock domain)
po_rx_reset	wire logic	output	Hardware/Software Global output reset (receive clock domain)
pi_power_off	wire logic	input	Power OFF Power off (all internal clocks are disabled)
pi_mdio_clock	wire logic	input	Clocks MDIO clock used by the MDIO module

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Table 15 – continued from previous page

Name	Type	Direction	Description
pi_host_clock	wire logic	input	HOST clock used by the reset synchronization block
pi_host_clock_en	wire logic	input	HOST clock enable
pi_ref_clock	wire logic	input	125 MHz Reference Clock
po_gtx_clock	wire logic	output	GMII Transmit clock (balanced with the EMAC internal clock)
pi_tx_clock	wire logic	input	Transmit 25/2.5 MHz Clock (from PHY)
pi_tx_clock_en	wire logic [3 : 0]	input	Enable Transmit 25/2.5 MHz Clock (from PHY)
pi_rx_clock	wire logic	input	Receive 125/25/2.5 MHz Clock (from PHY)
pi_rx_clock_en	wire logic [2 : 0]	input	Enable Receive 125/25/2.5 MHz Clock (from PHY)
pi_loopback	wire logic	input	Operating Mode Information MUX clock domain to TX Clock domain
pi_gigabit	wire logic	input	Clocks divider/MUX information
po_mdio_clock_f	wire logic	output	Output MDIO clock MDIO clock used by the MDIO module
po_host_clock_f	wire logic	output	Output Host Clock Host Free Clock
po_host_clock_g	wire logic	output	Host Gated Clock
po_tx_clock_f	wire logic	output	Output Transmit Clocks Transmit Free 125/25/12.5 MHz Clock for external interface
po_tx_clock_g	wire logic [3 : 0]	output	po_tx_clock_if , // Transmit Inverted Free 125/25/12.5 MHz Clock for external interface Transmit Gated 125/25/12.5 MHz Clock for external interface
po_rx_clock_f	wire logic	output	Output Receive Clocks Receive Free 125/25/12.5 MHz clock for external interface
po_rx_clock_g	wire logic [2 : 0]	output	Receive Gated 125/25/12.5 MHz clock for external interface
pi_test_en	wire logic	input	Test and Scan interface signals Test enable (test clock select)

continues on next page

Table 15 – continued from previous page

Name	Type	Direction	Description
pi_bistmode_en	wire logic	input	

Instances

ip_emac_top : *ip_emac_top*
↪mac_top : *ip_mac_top_g*
↪mac_clk_mng : *ip_mac_clk_mng_g*

Submodules

ip_mac_clk_mng_g
↪gtx_clock_out : *ip_gate_clock_g*
↪host_free_clock : *ip_gate_clock_g*
↪host_gate_clock_1 : *ip_gate_clock_g*
↪host_sreset : *ip_sync_reset_g*
↪hw_host_sreset : *ip_sync_reset_g*
↪mdio_free_clock : *ip_gate_clock_g*
↪mdio_sreset : *ip_sync_reset_g*
↪rx_free_clock : *ip_gate_clock_g*
↪rx_gate_clock_1 : *ip_gate_clock_g*
↪rx_gate_clock_2 : *ip_gate_clock_g*
↪rx_gate_clock_3 : *ip_gate_clock_g*
↪rx_sreset : *ip_sync_reset_g*
↪tx_free_clock : *ip_gate_clock_g*
↪tx_gate_clock_1 : *ip_gate_clock_g*
↪tx_gate_clock_2 : *ip_gate_clock_g*
↪tx_gate_clock_3 : *ip_gate_clock_g*
↪tx_gate_clock_4 : *ip_gate_clock_g*
↪tx_sreset : *ip_sync_reset_g*

6.12 Module ip_mac_dram_001

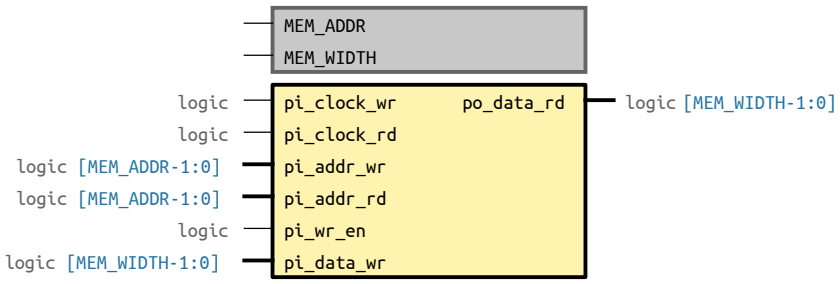

Fig. 12: Block Diagram of ip_mac_dram_001

Overview

The internal DRAM memory modules have the property that when the read address selects a memory location, this location is write protected (locked for write operation). Since when FIFO is empty both read and write addresses points to the same address and the a write operation should be performed, the read memory address should point to an unused memory location in order to unlock the write operation. Moving the internal address to an unused location when write enable modifies the read operation timing since the read DRAM address does not point to the right read address. In order to avoid the timing read response delay a bypass register between input and output data is used. When FIFO is empty the output data reads the bypass register instead of DRAM memory output.

Note: No bypass is necessary for Hash table memory since the read is not performed in the same time memory is writed. Bypass data register and bypass select multiplexer is removed from this module

Table 16: Parameters

Name	Default	Description
MEM_ADDR	9	Address width (9 -> 512 locations, 10->1024)
MEM_WIDTH	39	Data width

Table 17: Ports

Name	Type	Direction	Description
pi_clock_wr	wire logic	input	Input write clock (multiplexed with scan clock ouside this module)
pi_clock_rd	wire logic	input	Input read clock
pi_addr_wr	wire logic [*MEM_ADDR* - 1 : 0]	input	Write address
pi_addr_rd	wire logic [*MEM_ADDR* - 1 : 0]	input	Read address
pi_wr_en	wire logic	input	Write enable
pi_data_wr	wire logic [*MEM_WIDTH* - 1 : 0]	input	Write data

continues on next page

Table 17 – continued from previous page

Name	Type	Direction	Description
po_data_rd	wire logic [*MEM_WIDTH* - 1 : 0]	output	Read data

Always Blocks

always@(pi_wr_en or pi_addr_rd or pi_addr_wr)

Read Pointer Move (when read pointer equal write pointer and write enable the read memory address should not point to the writed location)

Instances

ip_emac_top : *ip_emac_top*
↪mac_top : *ip_mac_top_g*
↪mac_tx_top : *ip_mac_tx_top_g*
↪tx_data_dram : *ip_mac_dram_001* #(.MEM_ADDR(10), .MEM_WIDTH(39))

Submodules

ip_mac_dram_001 #(.MEM_ADDR(10), .MEM_WIDTH(39))
↪dram_001 : *dram_001* #(.MEM_ADDR(10), .MEM_WIDTH(39))

6.13 Module ip_mac_dram_002

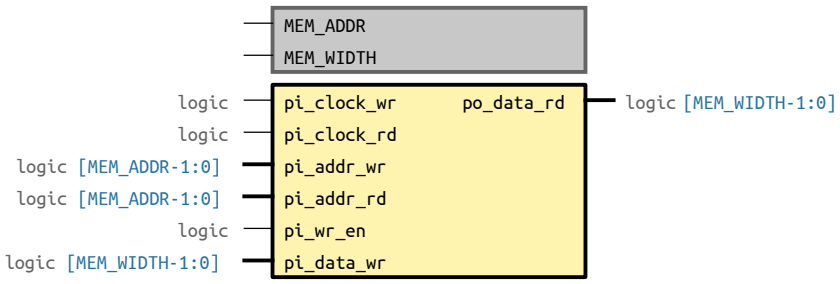

Fig. 13: Block Diagram of ip_mac_dram_002

Overview

The internal DRAM memory modules have the property that when the read address selects a memory location, this location is write protected (locked for write operation). Since when FIFO is empty both read and write addresses points to the same address and the a write operation should be performed, the read memory address should point to an unused memory location in order to unlock the write operation. Moving the internal address to an unused location when write enable modifies the read operation timing since the read DRAM address does not point to the right read address. In order to avoid the timing read response delay a bypass register between input and output data is used. When FIFO is empty the output data reads the bypass register instead of DRAM memory output.

Note: No bypass is necessary for Hash table memory since the read is not performed in the same time memory is writed. Bypass data register and bypass select multiplexer is removed from this module

Table 18: Parameters

Name	Default	Description
MEM_ADDR	9	Address width (9 -> 512 locations, 10->1024)
MEM_WIDTH	37	Data width

Table 19: Ports

Name	Type	Direction	Description
pi_clock_wr	wire logic	input	Input write clock (multiplexed with scan clock ouside this module)
pi_clock_rd	wire logic	input	Input read clock
pi_addr_wr	wire logic [*MEM_ADDR* - 1 : 0]	input	Write address
pi_addr_rd	wire logic [*MEM_ADDR* - 1 : 0]	input	Read address
pi_wr_en	wire logic	input	Write enable
pi_data_wr	wire logic [*MEM_WIDTH* - 1 : 0]	input	Write data

continues on next page

Table 19 – continued from previous page

Name	Type	Direction	Description
po_data_rd	wire logic [*MEM_WIDTH* - 1 : 0]	output	Read data

Always Blocks

always@(pi_wr_en or pi_addr_rd or pi_addr_wr)

Read Pointer Move (when read pointer equal write pointer and write enable the read memory address should not point to the writed location

Instances

ip_emac_top : *ip_emac_top*
↪mac_top : *ip_mac_top_g*
↪mac_rx_top : *ip_mac_rx_top_g*
↪rx_data_dram : *ip_mac_dram_002* #(.MEM_ADDR(10), .MEM_WIDTH(37))

Submodules

ip_mac_dram_002 #(.MEM_ADDR(10), .MEM_WIDTH(37))
↪dram_001 : *dram_001* #(.MEM_ADDR(10), .MEM_WIDTH(37))

6.14 Module ip_mac_dram_003

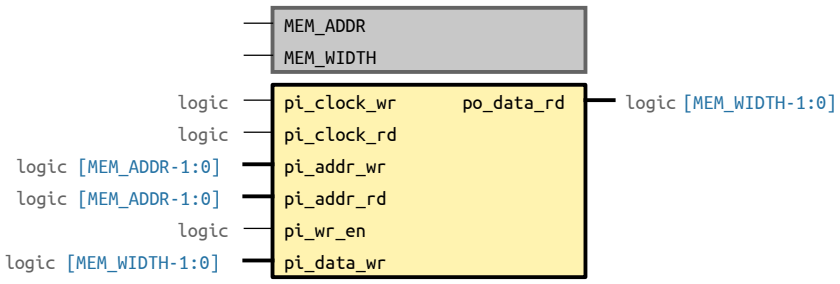

Fig. 14: Block Diagram of ip_mac_dram_003

Overview

The internal DRAM memory modules have the property that when the read address selects a memory location, this location is write protected (locked for write operation). Since when FIFO is empty both read and write addresses points to the same address and the a write operation should be performed, the read memory address should point to an unused memory location in order to unlock the write operation. Moving the internal address to an unused location when write enable modifies the read operation timing since the read DRAM address does not point to the right read address. In order to avoid the timing read response delay a bypass register between input and output data is used. When FIFO is empty the output data reads the bypass register instead of DRAM memory output.

Note: No bypass is necessary for Hash table memory since the read is not performed in the same time memory is writed. Bypass data register and bypass select multiplexer is removed from this module

Table 20: Parameters

Name	Default	Description
MEM_ADDR	4	Address width (9 -> 512 locations, 10->1024)
MEM_WIDTH	16	Data width

Table 21: Ports

Name	Type	Direction	Description
pi_clock_wr	wire logic	input	Input write clock (multiplexed with scan clock ouside this module)
pi_clock_rd	wire logic	input	Input read clock
pi_addr_wr	wire logic [*MEM_ADDR* - 1 : 0]	input	Write address
pi_addr_rd	wire logic [*MEM_ADDR* - 1 : 0]	input	Read address
pi_wr_en	wire logic	input	Write enable
pi_data_wr	wire logic [*MEM_WIDTH* - 1 : 0]	input	Write data

continues on next page

Table 21 – continued from previous page

Name	Type	Direction	Description
po_data_rd	wire logic [*MEM_WIDTH* - 1 : 0]	output	Read data

Always Blocks

always@(pi_wr_en or pi_addr_rd or pi_addr_wr)

Read Pointer Move (when read pointer equal write pointer and write enable the read memory address should not point to the writed location)

Instances

ip_emac_top : *ip_emac_top*
↪mac_top : *ip_mac_top_g*
↪mac_rx_top : *ip_mac_rx_top_g*
↪rx_dram_hash_1 : *ip_mac_dram_003* #(.MEM_ADDR(4), .MEM_WIDTH(16))

Submodules

ip_mac_dram_003 #(.MEM_ADDR(4), .MEM_WIDTH(16))
↪dram_001 : *dram_001* #(.MEM_ADDR(4), .MEM_WIDTH(16))

6.15 Module ip_mac_dram_004

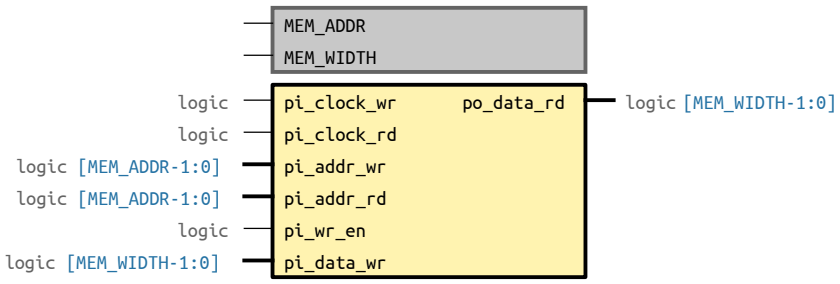

Fig. 15: Block Diagram of ip_mac_dram_004

Overview

The internal DRAM memory modules have the property that when the read address selects a memory location, this location is write protected (locked for write operation). Since when FIFO is empty both read and write addresses points to the same address and the a write operation should be performed, the read memory address should point to an unused memory location in order to unlock the write operation. Moving the internal address to an unused location when write enable modifies the read operation timing since the read DRAM address does not point to the right read address. In order to avoid the timing read response delay a bypass register between input and output data is used. When FIFO is empty the output data reads the bypass register instead of DRAM memory output.

Note: No bypass is necessary for Hash table memory since the read is not performed in the same time memory is writed. Bypass data register and bypass select multiplexer is removed from this module

Table 22: Parameters

Name	Default	Description
MEM_ADDR	4	Address width (9 -> 512 locations, 10->1024)
MEM_WIDTH	32	Data width

Table 23: Ports

Name	Type	Direction	Description
pi_clock_wr	wire logic	input	Input write clock (multiplexed with scan clock ouside this module)
pi_clock_rd	wire logic	input	Input read clock
pi_addr_wr	wire logic [*MEM_ADDR* - 1 : 0]	input	Write address
pi_addr_rd	wire logic [*MEM_ADDR* - 1 : 0]	input	Read address
pi_wr_en	wire logic	input	Write enable
pi_data_wr	wire logic [*MEM_WIDTH* - 1 : 0]	input	Write data

continues on next page

Table 23 – continued from previous page

Name	Type	Direction	Description
po_data_rd	wire logic [*MEM_WIDTH* - 1 : 0]	output	Read data

Always Blocks

`always@(pi_wr_en or pi_addr_rd or pi_addr_wr)`

Read Pointer Move (when read pointer equal write pointer and write enable the read memory address should not point to the writed location)

Instances

ip_emac_top : *ip_emac_top*
↪mac_top : *ip_mac_top_g*
↪mac_rx_top : *ip_mac_rx_top_g*
↪rx_dram_hash_0 : *ip_mac_dram_004* #(.MEM_ADDR(4), .MEM_WIDTH(32))

Submodules

ip_mac_dram_004 #(.MEM_ADDR(4), .MEM_WIDTH(32))
↪dram_001 : *dram_001* #(.MEM_ADDR(4), .MEM_WIDTH(32))

6.16 Module ip_mac_fc_dec_g

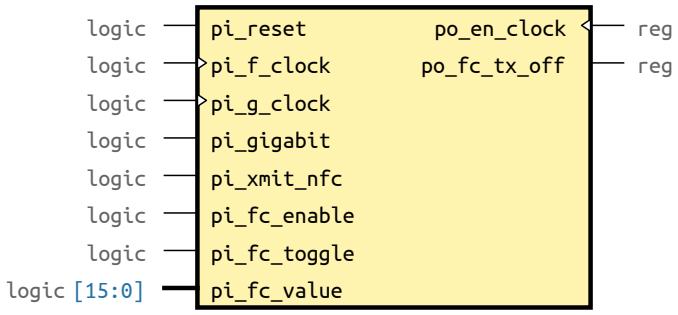

Fig. 16: Block Diagram of ip_mac_fc_dec_g

Table 24: Ports

Name	Type	Direction	Description
pi_reset	wire logic	input	Global Software/Hardware Reset (receive clock domain)
pi_f_clock	wire logic	input	Free Receive GMII/MII 125/25/2.5 MHz clock (from Clock Manager)
pi_g_clock	wire logic	input	Gated Receive GMII/MII 125/25/2.5 MHz clock (from Clock Manager)
po_en_clock	reg	output	Enable Receive GMII/MII 125/25/2.5 MHz clock (from Clock Manager)
pi_gigabit	wire logic	input	Operating 1000 Mbps (Gigabit) mode
pi_xmit_nfc	wire logic	input	Transmit FSM data frame transmit enable (when full duplex)
pi_fc_enable	wire logic	input	NOTE: This signal is not asserted during flow control frame transmission Receive flow control enable (flow control decoding enable)
pi_fc_toggle	wire logic	input	New pause frame received (pi_fc_value valid)
pi_fc_value	wire logic [15 : 0]	input	Pause time (from RX EMAC, FC frame decoding)
po_fc_tx_off	reg	output	Received FC packet (Transmit stop command)

Always Blocks

`always@(posedge pi_g_clock or negedge pi_reset)`
: FC Transmit OFF Process

`always@(posedge pi_f_clock or negedge pi_reset)`
: Clock Gating Module

Instances

ip_emac_top : *ip_emac_top*
↪mac_top : *ip_mac_top_g*
↪mac_rx_top : *ip_mac_rx_top_g*
↪fc_dec : *ip_mac_fc_dec_g*

6.17 Module ip_mac_fc_gen_g

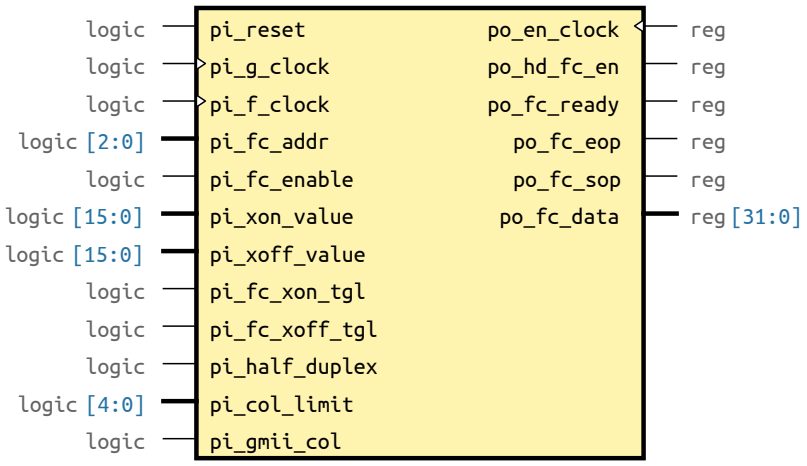

Fig. 17: Block Diagram of ip_mac_fc_gen_g

Overview

The flow control (PAUSE) operation is used to inhibit transmission of data frames for a specified period of time. A MAC Control client wishing to inhibit transmission of data frames from another station on the network generates a MAC CONTROL frame specifying: - The globally assigned 48-bit multicast destination address 01-80-C2-00-00-01H - The PAUSE opcode 00-01H - The CONTROL frame type 88-08H - A request Pause Value (16-bit value) indicating the length of time for which it wishes to inhibit data frame transmission.

The PAUSE operation cannot be used to inhibit transmission of MAC Control frames. PAUSE frames shall only be sent by MAC's configured to the full duplex mode of operation. The globally assigned 48-bit multicast address 01-80-C2-00-00-01 has been reserved for use in MAC Control PAUSE frames for inhibiting transmission of data frames from a MAC in a full duplex mode.

Table 25: Ports

Name	Type	Direction	Description
pi_reset	wire logic	input	Global Hardware/Software reset (active low)
pi_g_clock	wire logic	input	Transmit GMII/MII 125/25/2.5 MHz clock (from Clock Manager, gated clock)
pi_f_clock	wire logic	input	Transmit GMII/MII 125/25/2.5 MHz clock (from Clock Manager, free clock)
po_en_clock	reg	output	Transmit GMII/MII 125/25/2.5 MHz clock gated clock enable
pi_fc_addr	wire logic [2 : 0]	input	Command interface Next FC word request (from TX state)
pi_fc_enable	wire logic	input	Enable flow control

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Table 25 – continued from previous page

Name	Type	Direction	Description
pi_xon_value	wire logic [15 : 0]	input	from configuration XOFF flow control pause value
pi_xoff_value	wire logic [15 : 0]	input	from configuration XON flow control pause value
pi_fc_xon_tgl	wire logic	input	Request insert FC XON/XOFF (each time the following input toggle) from RX EMAC insert XOFF flow control information
pi_fc_xoff_tgl	wire logic	input	from RX EMAC insert XON flow control information
pi_half_duplex	wire logic	input	Half duplex flow control Operating in half duplex mode
pi_col_limit	wire logic [4 : 0]	input	Half duplex back pressure collision limit
pi_gmii_col	wire logic	input	Collision indication used to count the collisions during HD FC enable
po_hd_fc_en	reg	output	Half Duplex flow control enable
po_fc_ready	reg	output	FC frame interface Request to insert a new FC frame
po_fc_eop	reg	output	Note: When asserted has the meaning of ready and start of frame Flow control frame end of frame
po_fc_sop	reg	output	Flow control frame start of frame
po_fc_data	reg [31 : 0]	output	Flow control frame data

Always Blocks

`always@(posedge pi_g_clock or negedge pi_reset)`

Data Count Process

`always@(posedge pi_g_clock or negedge pi_reset)`

FC Data Out Process

`always@(posedge pi_f_clock or negedge pi_reset)`

Clock Gating Module

Instances

ip_emac_top : *ip_emac_top*
↪mac_top : *ip_mac_top_g*
↪mac_tx_top : *ip_mac_tx_top_g*
↪tx_fc_gen : *ip_mac_fc_gen_g*

6.18 Module ip_mac_host_if

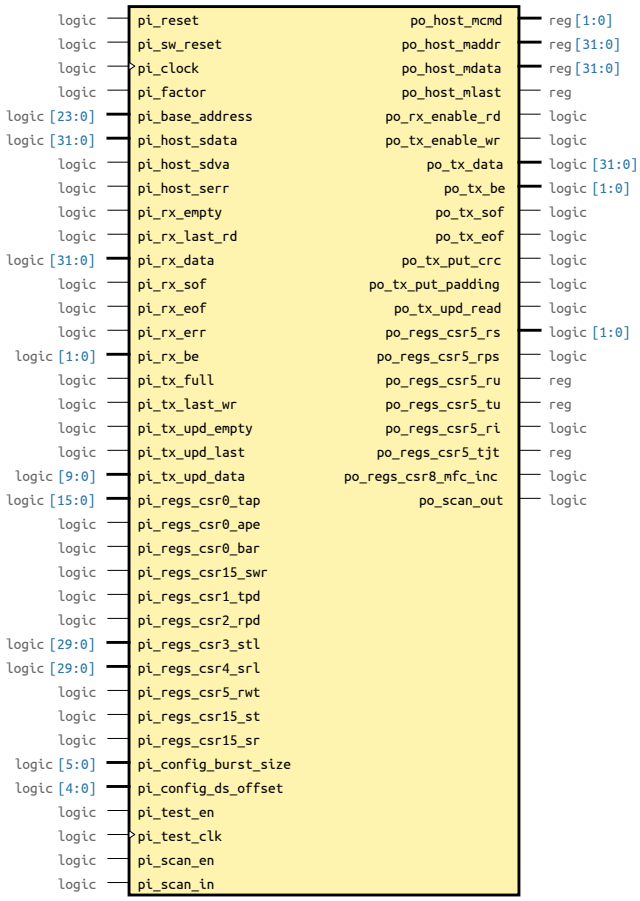

Fig. 18: Block Diagram of ip_mac_host_if

Table 26: Ports

Name	Type	Direction	Description
pi_reset	wire logic	input	Global interface global asynchronous reset
pi_sw_reset	wire logic	input	software reset
pi_clock	wire logic	input	host clock
pi_factor	wire logic	input	host clock enable
pi_base_address	wire logic [23 : 0]	input	HOST Interface device int mem space base address
po_host_mcmd	reg [1 : 0]	output	command
po_host_maddr	reg [31 : 0]	output	address
po_host_mdata	reg [31 : 0]	output	data to write

continues on next page

Table 26 – continued from previous page

Name	Type	Direction	Description
po_host_mlast	reg	output	last word
pi_host_sdata	wire logic [31 : 0]	input	data to read
pi_host_sdva	wire logic	input	data valid
pi_host_serr	wire logic	input	error during last transaction
po_rx_enable_rd	wire logic	output	RX FIFO interface rx fifo read command
pi_rx_empty	wire logic	input	rx fifo full
pi_rx_last_rd	wire logic	input	rx fifo almost full
pi_rx_data	wire logic [31 : 0]	input	rx fifo data
pi_rx_sof	wire logic	input	rx fifo eof
pi_rx_eof	wire logic	input	rx fifo eof
pi_rx_err	wire logic	input	rx fifo error
pi_rx_be	wire logic [1 : 0]	input	rx fifo data byte enable
po_tx_enable_wr	wire logic	output	rx fifo read command
pi_tx_full	wire logic	input	rx fifo full
pi_tx_last_wr	wire logic	input	rx fifo almost full
po_tx_data	wire logic [31 : 0]	output	rx fifo data
po_tx_be	wire logic [1 : 0]	output	tx fifo data byte enable
po_tx_sof	wire logic	output	tx fifo start of frame
po_tx_eof	wire logic	output	tx fifo end of frame
po_tx_put_crc	wire logic	output	put crc indication (valid only when sof=1)
po_tx_put_padding	wire logic	output	put padding indication (valid only when sof=1)
po_tx_upd_read	wire logic	output	TX update fifo interface
pi_tx_upd_empty	wire logic	input	
pi_tx_upd_last	wire logic	input	
pi_tx_upd_data	wire logic [9 : 0]	input	

continues on next page

Table 26 – continued from previous page

Name	Type	Direction	Description
pi_regs_csr0_tap	wire logic [15 : 0]	input	Registers bank interface tx automatic polling period CSR0[31:16]
pi_regs_csr0_ape	wire logic	input	tx auto polling enable CSR[15]
pi_regs_csr0_bar	wire logic	input	bus arbitration
pi_regs_csr15_swr	wire logic	input	software reset
pi_regs_csr1_tpd	wire logic	input	transmit poll demand
pi_regs_csr2_rpd	wire logic	input	receive poll demand
pi_regs_csr3_stl	wire logic [29 : 0]	input	transmit descriptor base address
pi_regs_csr4_srl	wire logic [29 : 0]	input	receive descriptor base address
po_regs_csr5_rs	wire logic [1 : 0]	output	receive process state
pi_regs_csr5_rwt	wire logic	input	receive watchdog timeout
po_regs_csr5_rps	wire logic	output	receive process stopped
po_regs_csr5_ru	reg	output	receive buffer unavailable
po_regs_csr5_tu	reg	output	transmit buffer unavailable
po_regs_csr5_ri	wire logic	output	receive interupt
po_regs_csr5_tjt	reg	output	signals Transmit jabber timeout error to the CSR5 register; this will signal to the HOST to perform a software reset to the EMAC
pi_regs_csr15_st	wire logic	input	start/stop transmit
pi_regs_csr15_sr	wire logic	input	start / stop receive
po_regs_csr8_mfc_inc	wire logic	output	missed frame counter increment command
pi_config_burst_size	wire logic [5 : 0]	input	limit for the rx,tx burst transfers
pi_config_ds_offset	wire logic [4 : 0]	input	pi_rx_mac_ds_poll, //from the RX EMAC part (new frame arrived, or new data arrived) offset to increment the address if a descriptor
pi_test_en	wire logic	input	Test and Scan interface signals Test enable
pi_test_clk	wire logic	input	Test clock
pi_scan_en	wire logic	input	SCAN chain shift enable

continues on next page

Table 26 – continued from previous page

Name	Type	Direction	Description
pi_scan_in	wire logic	input	SCAN chain input
po_scan_out	wire logic	output	SCAN chain output

Always Blocks

always@(posedge clock or negedge reset)

Manages the next descriptor aquire when rx_ds_needed is asserted, asserts rx_ds_req when pi_host_arb_ds_dv is asserted load pi_host_arb_ds_data into current_ds_addr and deasserts po_host_arb_ds_req the one that asserted ds_needed waits for pi_host_arb_ds_dv to reset

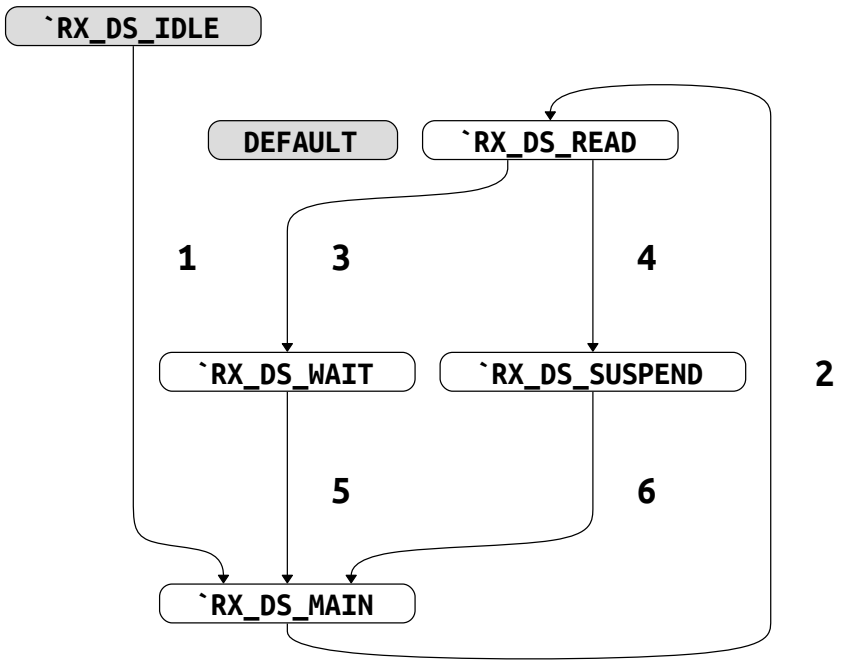

Table 27: FSM Transitions for rx_ds_state

#	Current State	Next State	Condition	Comment
1	`RX_DS_IDLE	`RX_DS_MAIN	[!(! pi_regs_csr15_sr)]	
2	`RX_DS_MAIN	`RX_DS_READ	[(rx_ds_allowed)]	
3	`RX_DS_READ	`RX_DS_WAIT	[((pi_host_sdva) && (pi_host_-sdata[31]))]	
4	`RX_DS_READ	`RX_DS_SUS-PEND	[((pi_host_sdva) && !(pi_host_-sdata[31]))]	
5	`RX_DS_WAIT	`RX_DS_MAIN	[(rx_valid_ds_read)]	
6	`RX_DS_SUS-PEND	`RX_DS_MAIN	[(rx_mac_ds_poll || pi_regs_csr2_-rpd)]	

always@(posedge clock or negedge reset)

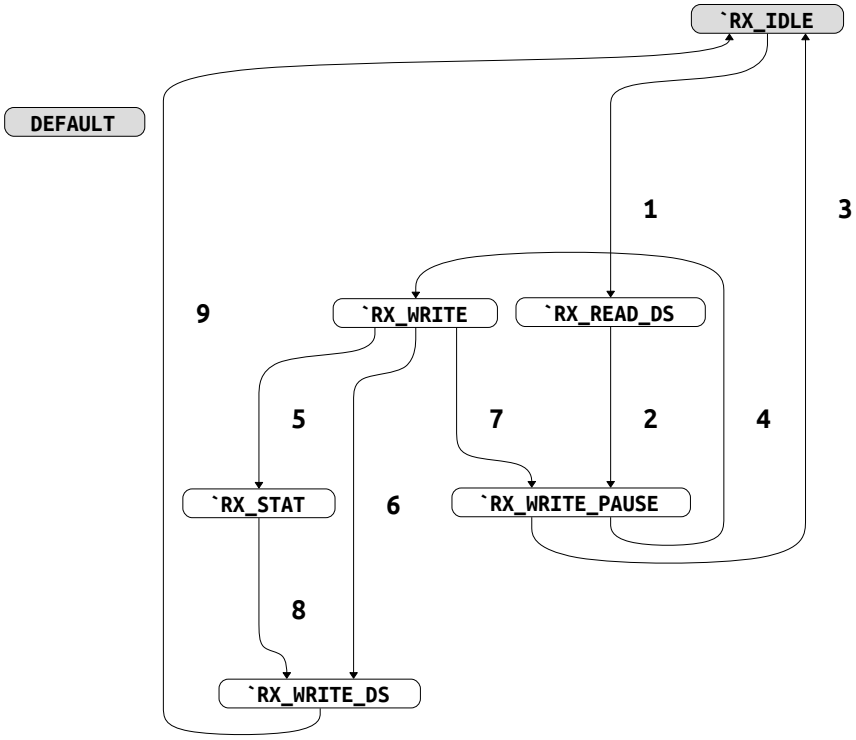

Table 28: FSM Transitions for rx_state

#	Current State	Next State	Condition	Comment
1	`RX_IDLE	`RX_READ_DS	[(rx_allowed)]	
2	`RX_READ_DS	`RX_WRITE_-PAUSE	[((pi_host_sdva) && !(rx_burst_cnt == 0) && !(rx_burst_cnt == 1) && (rx_burst_cnt == 2))]	
3	`RX_WRITE_-PAUSE	`RX_IDLE	[(! rx_ds_valid)]	
4	`RX_WRITE_-PAUSE	`RX_WRITE	[(!(! rx_ds_valid) && !(! pi_rx_-empty && ! pi_rx_last_rd && ! rx_-req) && (rx_allowed))]	
5	`RX_WRITE	`RX_STAT	[(!(rx_first_word_in_burst) && !(! pi_host_sdva) && (rx_mlast) && (rx_frame_complete))]	
6	`RX_WRITE	`RX_WRITE_DS	[(!(rx_first_word_in_burst) && !(! pi_host_sdva) && (rx_mlast) && !(rx_frame_complete) && (rx_-buff_complete) && !(! rx_cur_buff && ! rx_ds1[24] && rx_ds1[21 : 11] != 0))]	

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Table 28 – continued from previous page

#	Current State	Next State	Condition	Comment
7	`RX_WRITE	`RX_WRITE_PAUSE	[(!(rx_first_word_in_burst) && !(! pi_host_sdva) && (rx_mlast) && !(rx_frame_complete) && !(rx_buff_complete) && (rx_burst_complete)), (!(rx_first_word_in_burst) && !(! pi_host_sdva) && (rx_mlast) && !(rx_frame_complete) && !(rx_buff_complete) && !(rx_burst_complete)), (!(rx_first_word_in_burst) && !(! pi_host_sdva) && (rx_mlast) && !(rx_frame_complete) && (rx_buff_complete) && (! rx_cur_buff && ! rx_ds1[24] && rx_ds1[21 : 11] != 0))]	
8	`RX_STAT	`RX_WRITE_DS	[(! pi_rx_empty)]	
9	`RX_WRITE_DS	`RX_IDLE	[(rx_allowed && pi_host_sdva)]	

always@(posedge clock or negedge reset)

Manages the next descriptor aquire

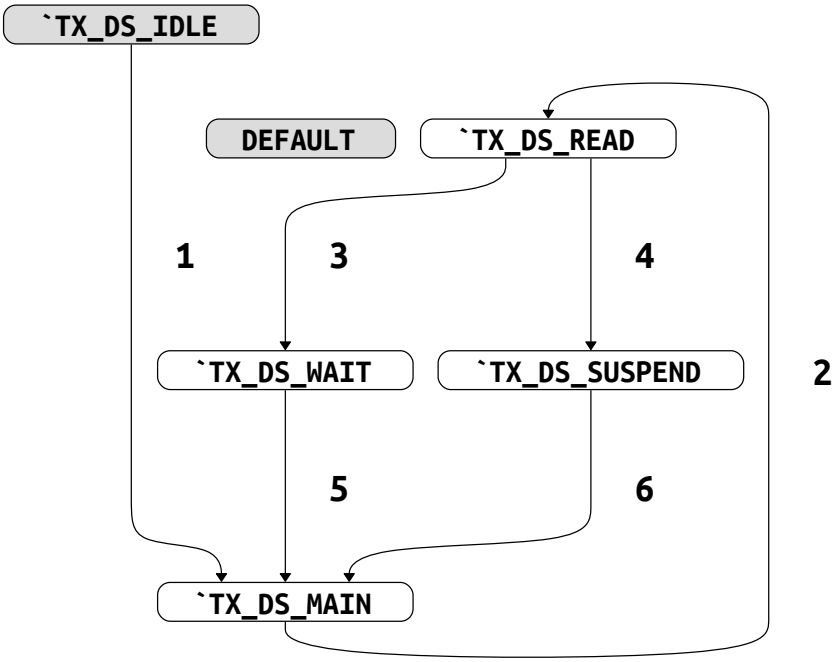

Table 29: FSM Transitions for tx_ds_state

#	Current State	Next State	Condition	Comment
1	`TX_DS_IDLE	`TX_DS_MAIN	[!(! pi_regs_csr15_st)]	
2	`TX_DS_MAIN	`TX_DS_READ	[(tx_ds_allowed)]	
3	`TX_DS_READ	`TX_DS_WAIT	[((pi_host_sdva) && (pi_host_sdata[31]))]	
4	`TX_DS_READ	`TX_DS_SUSPEND	[((pi_host_sdva) && !(pi_host_sdata[31]))]	
5	`TX_DS_WAIT	`TX_DS_MAIN	[(tx_valid_ds_read)]	

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Table 29 – continued from previous page

#	Current State	Next State	Condition	Comment
6	`TX_DS_SUS-PEND	`TX_DS_MAIN	[(pi_regs_csr0_ape && tx_ds_poll_-cnt == pi_regs_csr0_tap || pi_regs_-csr1_tpd)]	

```
always@(posedge clock or negedge reset)
```

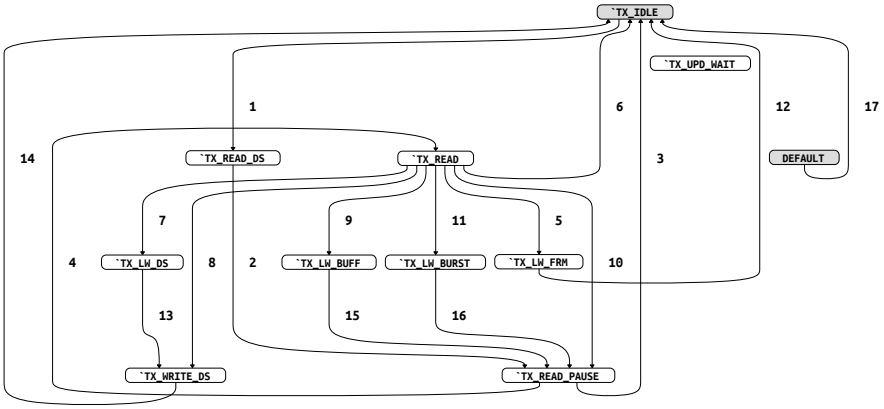

Table 30: FSM Transitions for tx_state

#	Current State	Next State	Condition	Comment
1	`TX_IDLE	`TX_READ_DS	[(!(! pi_regs_csr15_st) && !(tx_ds_-addr_valid && ! pi_tx_full && ! pi_tx_last_wr && ! tx_upd_fifo_full && ! tx_req) && (tx_allowed))]	
2	`TX_READ_DS	`TX_READ_-PAUSE	[((pi_host_sdva) && !(tx_burst_cnt == 0) && !(tx_burst_cnt == 1) && (tx_burst_cnt == 2))]	
3	`TX_READ_-PAUSE	`TX_IDLE	[(! tx_ds_valid)]	
4	`TX_READ_-PAUSE	`TX_READ	[(!(! tx_ds_valid) && !(! pi_tx_full && ! pi_tx_last_wr && ! tx_req) && (tx_allowed))]	
5	`TX_READ	`TX_LW_FRM	[((pi_host_sdva) && (tx_mlast1) && (tx_word_cnt >= 16'h1000) && (pi_tx_last_wr)), ((pi_host_sdva) && (tx_mlast1) && !(tx_word_cnt >= 16'h1000) && (tx_buff_cnt == tx_curr_buff_size - 1) && (tx_-cur_buff || tx_ds1[24] || tx_ds1[21 : 11] == 0) && (tx_ds1[30]) && (pi_tx_last_wr))]	
6	`TX_READ	`TX_IDLE	[((pi_host_sdva) && (tx_mlast1) && (tx_word_cnt >= 16'h1000) && !(pi_tx_last_wr)), ((pi_host_sdva) && (tx_mlast1) && !(tx_word_cnt >= 16'h1000) && (tx_buff_cnt == tx_curr_buff_size - 1) && (tx_-cur_buff || tx_ds1[24] || tx_ds1[21 : 11] == 0) && (tx_ds1[30]) && !(pi_tx_last_wr))]	

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Table 30 – continued from previous page

#	Current State	Next State	Condition	Comment
7	`TX_READ	`TX_LW_DS	[((pi_host_sdva) && (tx_mlast1) && !(tx_word_cnt >= 16'h1000) && (tx_buff_cnt == tx_curr_buff_size - 1) && (tx_cur_buff || tx_ds1[24] || tx_ds1[21 : 11] == 0) && !(tx_ds1[30]) && (pi_tx_last_wr))]	
8	`TX_READ	`TX_WRITE_DS	[((pi_host_sdva) && (tx_mlast1) && !(tx_word_cnt >= 16'h1000) && (tx_buff_cnt == tx_curr_buff_size - 1) && (tx_cur_buff || tx_ds1[24] || tx_ds1[21 : 11] == 0) && !(tx_ds1[30]) && !(pi_tx_last_wr))]	
9	`TX_READ	`TX_LW_BUFF	[((pi_host_sdva) && (tx_mlast1) && !(tx_word_cnt >= 16'h1000) && (tx_buff_cnt == tx_curr_buff_size - 1) && !(tx_cur_buff || tx_ds1[24] || tx_ds1[21 : 11] == 0) && (pi_tx_last_wr))]	
10	`TX_READ	`TX_READ_PAUSE	[((pi_host_sdva) && (tx_mlast1) && !(tx_word_cnt >= 16'h1000) && !(tx_buff_cnt == tx_curr_buff_size - 1) && (tx_burst_cnt == pi_config_burst_size - 1) && !(pi_tx_last_wr)), ((pi_host_sdva) && (tx_mlast1) && !(tx_word_cnt >= 16'h1000) && (tx_buff_cnt == tx_curr_buff_size - 1) && !(tx_cur_buff || tx_ds1[24] || tx_ds1[21 : 11] == 0) && !(pi_tx_last_wr))]	
11	`TX_READ	`TX_LW_BURST	[((pi_host_sdva) && !(tx_mlast1) && (pi_tx_last_wr || pi_tx_full)), ((pi_host_sdva) && (tx_mlast1) && !(tx_word_cnt >= 16'h1000) && !(tx_buff_cnt == tx_curr_buff_size - 1) && (tx_burst_cnt == pi_config_burst_size - 1) && (pi_tx_last_wr))]	
12	`TX_LW_FRM	`TX_IDLE	[!(pi_tx_last_wr)]	
13	`TX_LW_DS	`TX_WRITE_DS	[!(pi_tx_last_wr)]	
14	`TX_WRITE_DS	`TX_IDLE	[(pi_host_sdva)]	
15	`TX_LW_BUFF	`TX_READ_PAUSE	[!(pi_tx_last_wr)]	
16	`TX_LW_BURST	`TX_READ_PAUSE	[!(pi_tx_last_wr)]	
17	default	`TX_IDLE	[EMPTY]	Illegal state

`always@(posedge clock or negedge reset)`

Tx_upd_fifo holds data tx_upd_fifo_wa holds write address tx_upd_fifo_ra holds read address tx_state process write and increments tx_upd_fifo_wa tx_update_ds process read and increments tx_upd_fifo_ra

`always@(posedge clock or negedge reset)`

This process reads from both tx_upd_fifo and tx_upd_resp_fifo, constructs TX_RDS0 and assert tx_ds_req to arbiter along with address(tx_upd_fifo) and data (tx_upd_resp_fifo)

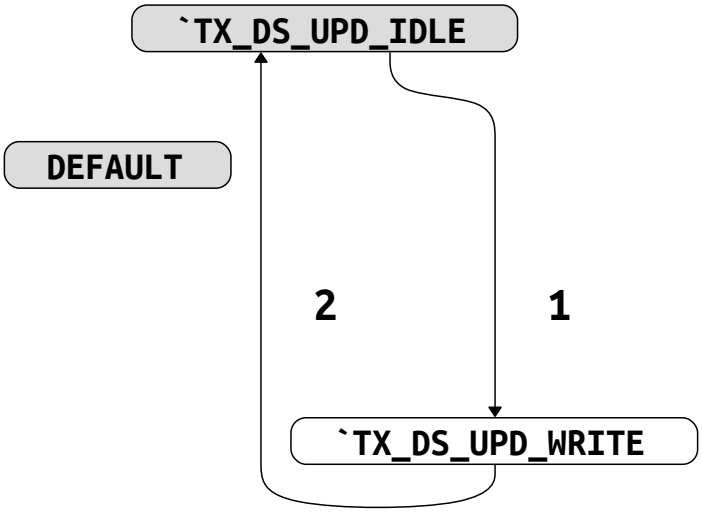

Table 31: FSM Transitions for tx_upd_state

#	Current State	Next State	Condition	Comment
1	`TX_DS_UPD_-IDLE	`TX_DS_UPD_-WRITE	[(tx_upd_req && tx_upd_allowed)]	
2	`TX_DS_UPD_-WRITE	`TX_DS_UPD_-IDLE	[(pi_host_sdva)]	

always@(posedge clock or negedge reset)

Process for arbiter

always@(arb_state or rx_req or tx_req or rx_ds_req or tx_ds_req or tx_upd_req)

Arbiter allowed calculation tx_frame_transmit

always@(arb_state or rx_allowed or tx_allowed or rx_ds_allowed or tx_ds_-allowed or tx_upd_allowed)

Arbiter next state calculation

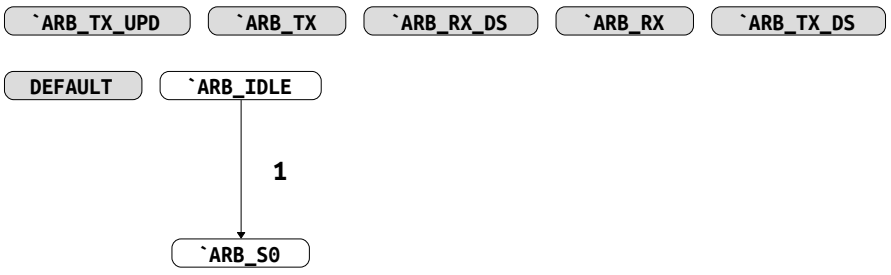

Table 32: FSM Transitions for arb_state

#	Current State	Next State	Condition	Comment
1	`ARB_IDLE	`ARB_S0	[(arb_enable)]	

always@(rx_allowed or tx_allowed or rx_ds_allowed or tx_ds_allowed or tx_upd_-allowed or rx_mcmd or rx_maddr or rx_mdata or rx_mlast or tx_mcmd or tx_maddr or tx_-mdata or tx_mlast or rx_ds_mcmd or rx_ds_maddr or rx_ds_mlast or tx_ds_mcmd or tx_ds_-maddr or tx_ds_mlast or tx_upd_mcmd or tx_upd_maddr or tx_upd_mdata or tx_upd_mlast)

Arbiter multiplexor

6.19 Module ip_mac_hostif_arb

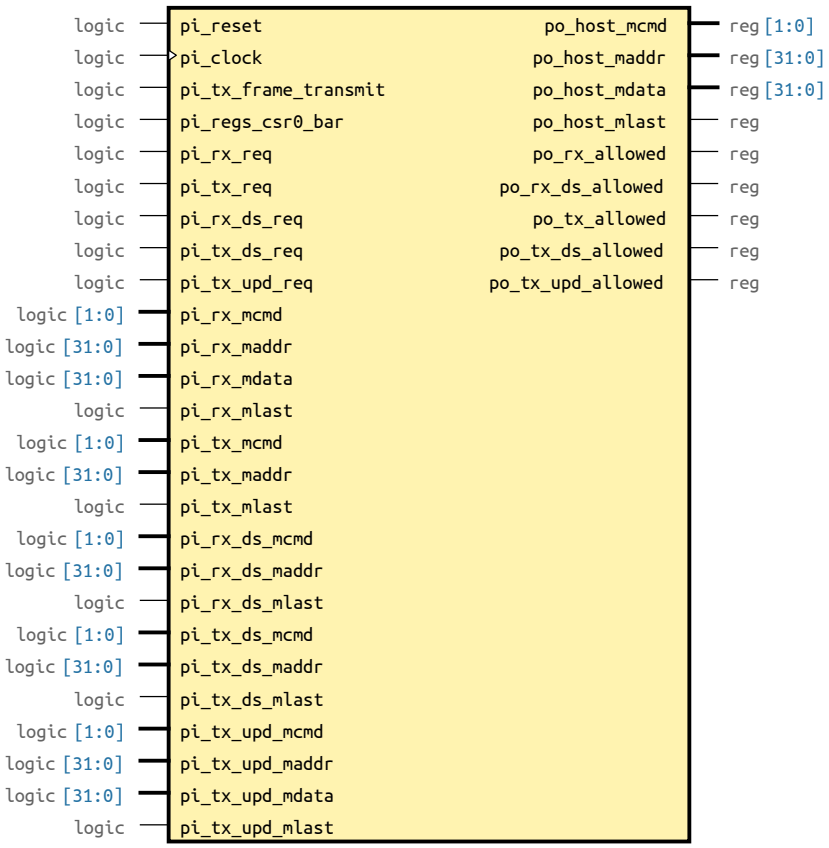

Fig. 19: Block Diagram of ip_mac_hostif_arb

Table 33: Ports

Name	Type	Direction	Description
pi_reset	wire logic	input	Global interface global asynchronous pi_reset
pi_clock	wire logic	input	host pi_clock
pi_tx_frame_transmit	wire logic	input	from pi_mac_hostif_tx
pi_regs_csr0_bar	wire logic	input	from banks regs
pi_rx_req	wire logic	input	
pi_tx_req	wire logic	input	
pi_rx_ds_req	wire logic	input	
pi_tx_ds_req	wire logic	input	
pi_tx_upd_req	wire logic	input	

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Table 33 – continued from previous page

Name	Type	Direction	Description
pi_rx_mcmd	wire logic [1 : 0]	input	
pi_rx_maddr	wire logic [31 : 0]	input	
pi_rx_mdata	wire logic [31 : 0]	input	
pi_rx_mlast	wire logic	input	
pi_tx_mcmd	wire logic [1 : 0]	input	
pi_tx_maddr	wire logic [31 : 0]	input	
pi_tx_mlast	wire logic	input	pi_tx_mdata,
pi_rx_ds_mcmd	wire logic [1 : 0]	input	
pi_rx_ds_maddr	wire logic [31 : 0]	input	
pi_rx_ds_mlast	wire logic	input	
pi_tx_ds_mcmd	wire logic [1 : 0]	input	
pi_tx_ds_maddr	wire logic [31 : 0]	input	
pi_tx_ds_mlast	wire logic	input	
pi_tx_upd_mcmd	wire logic [1 : 0]	input	
pi_tx_upd_maddr	wire logic [31 : 0]	input	
pi_tx_upd_mdata	wire logic [31 : 0]	input	
pi_tx_upd_mlast	wire logic	input	
po_host_mcmd	reg [1 : 0]	output	
po_host_maddr	reg [31 : 0]	output	
po_host_mdata	reg [31 : 0]	output	
po_host_mlast	reg	output	
po_rx_allowed	reg	output	
po_rx_ds_allowed	reg	output	
po_tx_allowed	reg	output	
po_tx_ds_allowed	reg	output	
po_tx_upd_allowed	reg	output	

Always Blocks

always@(posedge pi_clock or negedge pi_reset)

process for arbiter *

always@(arb_state or pi_rx_req or pi_tx_req or pi_rx_ds_req or pi_tx_ds_req or pi_tx_upd_req)

Arbiter allowed calculation pi_tx_frame_transmit

always@(arb_state or po_rx_allowed or po_tx_allowed or po_rx_ds_allowed or po_tx_ds_allowed or po_tx_upd_allowed)

Arbiter next state calculation

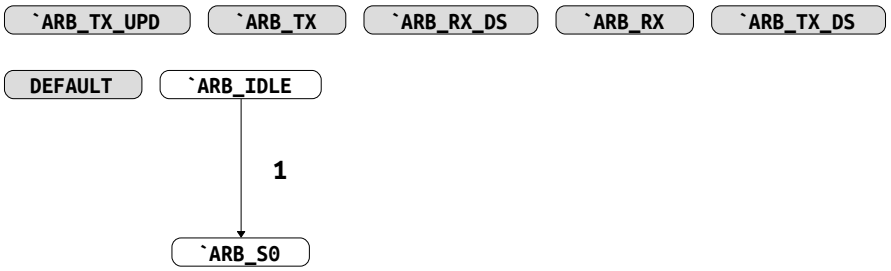

Table 34: FSM Transitions for arb_state

#	Current State	Next State	Condition	Comment
1	`ARB_IDLE	`ARB_S0	[!(~ pi_reset)]	

always@(po_rx_allowed or po_tx_allowed or po_rx_ds_allowed or po_tx_ds_allowed or po_tx_upd_allowed or pi_rx_mcmd or pi_rx_maddr or pi_rx_mdata or pi_rx_mlast or pi_tx_mcmd or pi_tx_maddr or pi_tx_mlast or pi_rx_ds_mcmd or pi_rx_ds_maddr or pi_rx_ds_mlast or pi_tx_ds_mcmd or pi_tx_ds_maddr or pi_tx_ds_mlast or pi_tx_upd_mcmd or pi_tx_upd_maddr or pi_tx_upd_mdata or pi_tx_upd_mlast)

Arbiter multiplexor

Instances

ip_emac_top : *ip_emac_top*
↪host_if : *ip_mac_hostif_top*
↪hostif_arb : *ip_mac_hostif_arb*

6.20 Module ip_mac_hostif_rx

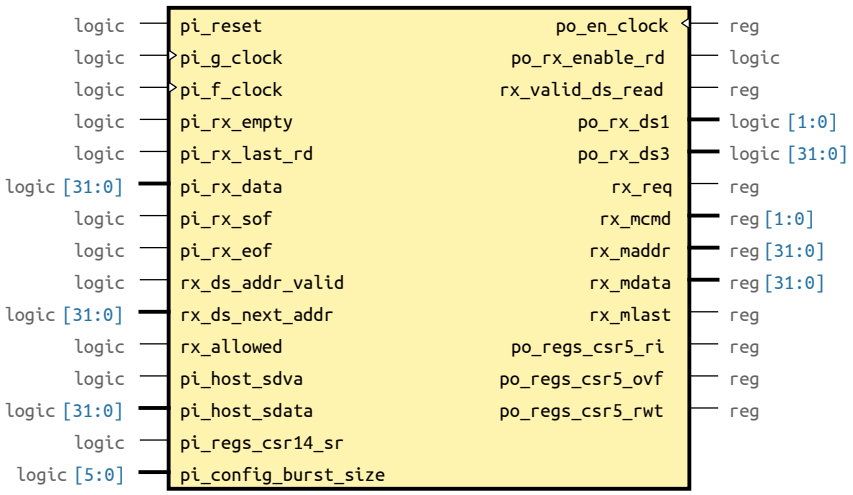

Fig. 20: Block Diagram of ip_mac_hostif_rx

Table 35: Ports

Name	Type	Direction	Description
pi_reset	wire logic	input	Global interface global asynchronous pi_reset
pi_g_clock	wire logic	input	host gated clock
pi_f_clock	wire logic	input	host free clock
po_en_clock	reg	output	enable clock condition
po_rx_enable_rd	wire logic	output	RX FIFO interface rx fifo read command
pi_rx_empty	wire logic	input	rx fifo full
pi_rx_last_rd	wire logic	input	rx fifo almost full
pi_rx_data	wire logic [31 : 0]	input	rx fifo data
pi_rx_sof	wire logic	input	rx fifo eof
pi_rx_eof	wire logic	input	rx fifo eof
rx_ds_addr_valid	wire logic	input	ip_mac_hostif_rxds from ip_mac_hostif_rxds (currently fetched descriptor address valid)
rx_ds_next_addr	wire logic [31 : 0]	input	from ip_mac_hostif_rxds (currently fetched descriptor address)
rx_valid_ds_read	reg	output	

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Table 35 – continued from previous page

Name	Type	Direction	Description
po_rx_ds1	wire logic [1 : 0]	output	mapped to rx, rx_ds1[25:24]
po_rx_ds3	wire logic [31 : 0]	output	
rx_req	reg	output	arbiter
rx_allowed	wire logic	input	
rx_mcmd	reg [1 : 0]	output	
rx_maddr	reg [31 : 0]	output	
rx_mdata	reg [31 : 0]	output	
rx_mlast	reg	output	
pi_host_sdva	wire logic	input	host interface
pi_host_sdata	wire logic [31 : 0]	input	
pi_regs_csr14_sr	wire logic	input	ip_mac_regs_bank (config)
pi_config_burst_size	wire logic [5 : 0]	input	limit for the rx,tx burst transfers
po_regs_csr5_ri	reg	output	
po_regs_csr5_ovf	reg	output	
po_regs_csr5_rwt	reg	output	

Always Blocks

`always@(posedge pi_g_clock or negedge pi_reset)`

state machine for rx descriptor based transfer

`always@(posedge pi_f_clock or negedge pi_reset)`

Gated Clock Enable

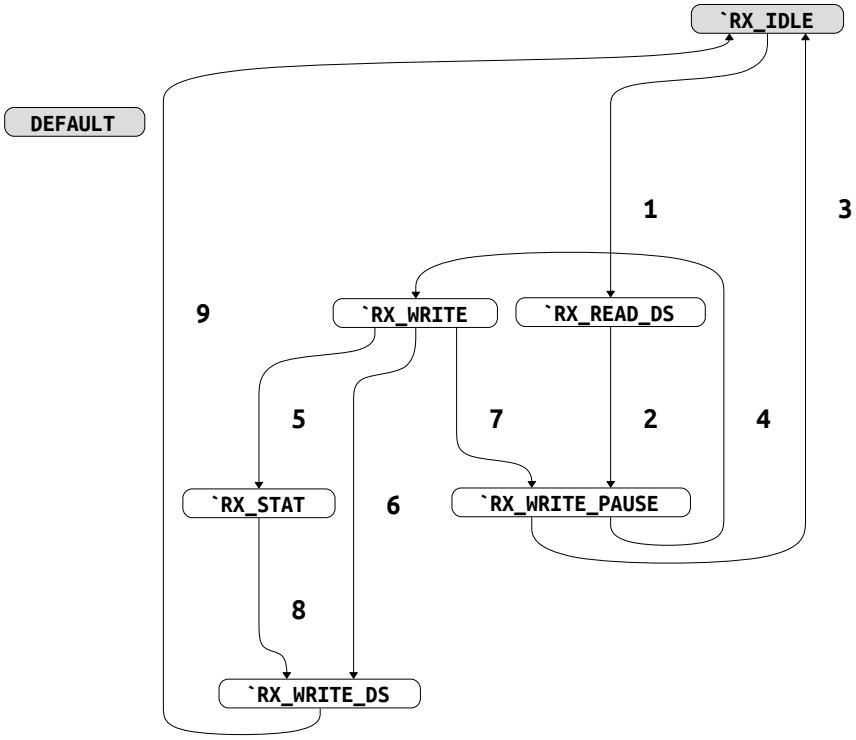

Table 36: FSM Transitions for rx_state

#	Current State	Next State	Condition	Comment
1	`RX_IDLE	`RX_READ_DS	[(!(~ pi_reset) && !(! rx_ds_addr_valid) && !(rx_ds_addr_valid && ! rx_req) && (rx_allowed))]	
2	`RX_READ_DS	`RX_WRITE_PAUSE	[(!(~ pi_reset) && (pi_host_sdva) && !(rx_burst_cnt == 0) && !(rx_burst_cnt == 1) && (rx_burst_cnt == 2))]	
3	`RX_WRITE_PAUSE	`RX_IDLE	[(!(~ pi_reset) && (! rx_ds_valid))]	
4	`RX_WRITE_PAUSE	`RX_WRITE	[(!(~ pi_reset) && !(! rx_ds_valid) && !(! pi_rx_empty && ! pi_rx_last_rd && ! rx_req) && (rx_allowed))]	
5	`RX_WRITE	`RX_STAT	[(!(~ pi_reset) && !(rx_first_word_in_burst) && !(! pi_host_sdva) && (rx_mlast) && (rx_frame_complete))]	
6	`RX_WRITE	`RX_WRITE_DS	[(!(~ pi_reset) && !(rx_first_word_in_burst) && !(! pi_host_sdva) && (rx_mlast) && !(rx_frame_complete) && (rx_buff_complete) && !(! rx_cur_buff && ! rx_ds1[24] && rx_ds1[21 : 11] != 0))]	

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Table 36 – continued from previous page

#	Current State	Next State	Condition	Comment
7	`RX_WRITE	`RX_WRITE_PAUSE	[(!(~ pi_reset) && !(rx_first_word_in_burst) && !(! pi_host_sdva) && (rx_mlast) && !(rx_frame_complete) && !(rx_buff_complete) && (rx_burst_complete)), (!(~ pi_reset) && !(rx_first_word_in_burst) && !(! pi_host_sdva) && (rx_mlast) && !(rx_frame_complete) && !(rx_buff_complete) && !(rx_burst_complete)), (!(~ pi_reset) && !(rx_first_word_in_burst) && !(! pi_host_sdva) && (rx_mlast) && !(rx_frame_complete) && (rx_buff_complete) && (! rx_cur_buff && ! rx_ds1[24] && rx_ds1[21 : 11] != 0))]	
8	`RX_STAT	`RX_WRITE_DS	[(!(~ pi_reset) && (! pi_rx_empty))]	
9	`RX_WRITE_DS	`RX_IDLE	[(!(~ pi_reset) && (rx_allowed && pi_host_sdva))]	

Instances

ip_emac_top : *ip_emac_top*
↪host_if : *ip_mac_hostif_top*
↪hostif_rx : *ip_mac_hostif_rx*

6.21 Module ip_mac_hostif_rxds

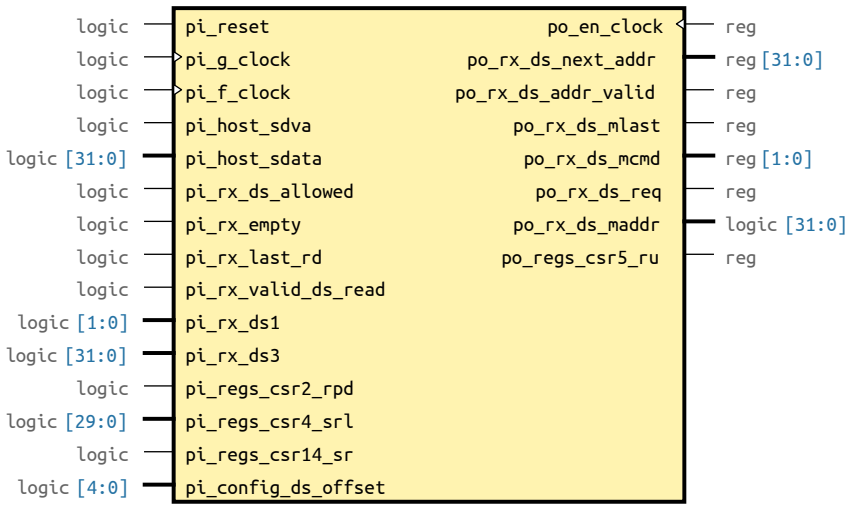

Fig. 21: Block Diagram of ip_mac_hostif_rxds

Table 37: Ports

Name	Type	Direction	Description
pi_reset	wire logic	input	Global interface global asynchronous pi_reset
pi_g_clock	wire logic	input	host gated clock
pi_f_clock	wire logic	input	host free clock
po_en_clock	reg	output	enable clock condition
pi_host_sdva	wire logic	input	
pi_host_sdata	wire logic [31 : 0]	input	mapped to pi_host_sdata[31]
pi_rx_ds_allowed	wire logic	input	
pi_rx_empty	wire logic	input	
pi_rx_last_rd	wire logic	input	
po_rx_ds_next_addr	reg [31 : 0]	output	output
po_rx_ds_addr_valid	reg	output	output
po_rx_ds_mlast	reg	output	output
po_rx_ds_mcmd	reg [1 : 0]	output	output
po_rx_ds_req	reg	output	output

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Table 37 – continued from previous page

Name	Type	Direction	Description
po_rx_ds_maddr	wire logic [31 : 0]	output	output
pi_rx_valid_ds_read	wire logic	input	input
pi_rx_ds1	wire logic [1 : 0]	input	holds current rx descriptor body mapped to rx, pi_rx_ds1[25:24]
pi_rx_ds3	wire logic [31 : 0]	input	
pi_regs_csr2_rpd	wire logic	input	Registers bank interface receive poll demand
pi_regs_csr4_srl	wire logic [29 : 0]	input	receive descriptor base address
po_regs_csr5_ru	reg	output	receive buffer unavailable
pi_regs_csr14_sr	wire logic	input	start / stop receive
pi_config_ds_offset	wire logic [4 : 0]	input	offset to increment the address if a descriptor

Always Blocks

`always@(posedge pi_g_clock or negedge pi_reset)`

Manages the next descriptor aquire when rx_ds_needed is asserted, asserts po_rx_ds_req when pi_host_arb_ds_dv is asserted load pi_host_arb_ds_data into current_ds_addr and deasserts po_host_arb_ds_req the one that asserted ds_needed waits for pi_host_arb_ds_dv to pi_reset

`always@(posedge pi_f_clock or negedge pi_reset)`

Gated Clock Enable

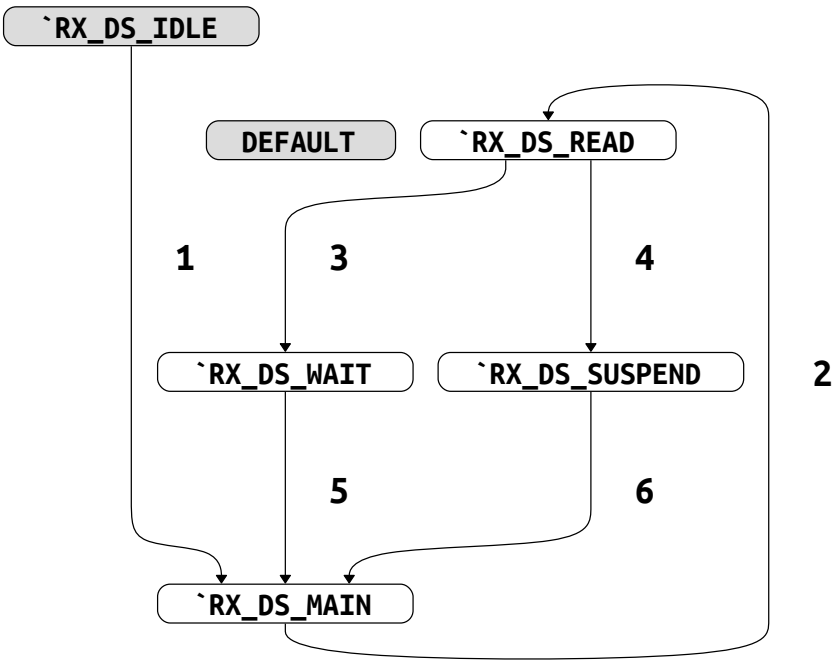

Table 38: FSM Transitions for rx_ds_state

#	Current State	Next State	Condition	Comment
1	`RX_DS_IDLE	`RX_DS_MAIN	[(!(~ pi_reset) && !(! pi_regs_csr14_sr))]	
2	`RX_DS_MAIN	`RX_DS_READ	[(!(~ pi_reset) && (pi_rx_ds_allowed))]	
3	`RX_DS_READ	`RX_DS_WAIT	[(!(~ pi_reset) && (pi_host_sdva) && (pi_host_sdata))]	
4	`RX_DS_READ	`RX_DS_SUSPEND	[(!(~ pi_reset) && (pi_host_sdva) && !(pi_host_sdata))]	
5	`RX_DS_WAIT	`RX_DS_MAIN	[(!(~ pi_reset) && (pi_rx_valid_ds_read))]	
6	`RX_DS_SUSPEND	`RX_DS_MAIN	[(!(~ pi_reset) && (rx_mac_ds_poll || pi_regs_csr2_rpd))]	

Instances

ip_emac_top : *ip_emac_top*
↪host_if : *ip_mac_hostif_top*
↪hostif_rxds : *ip_mac_hostif_rxds*

6.22 Module ip_mac_hostif_top

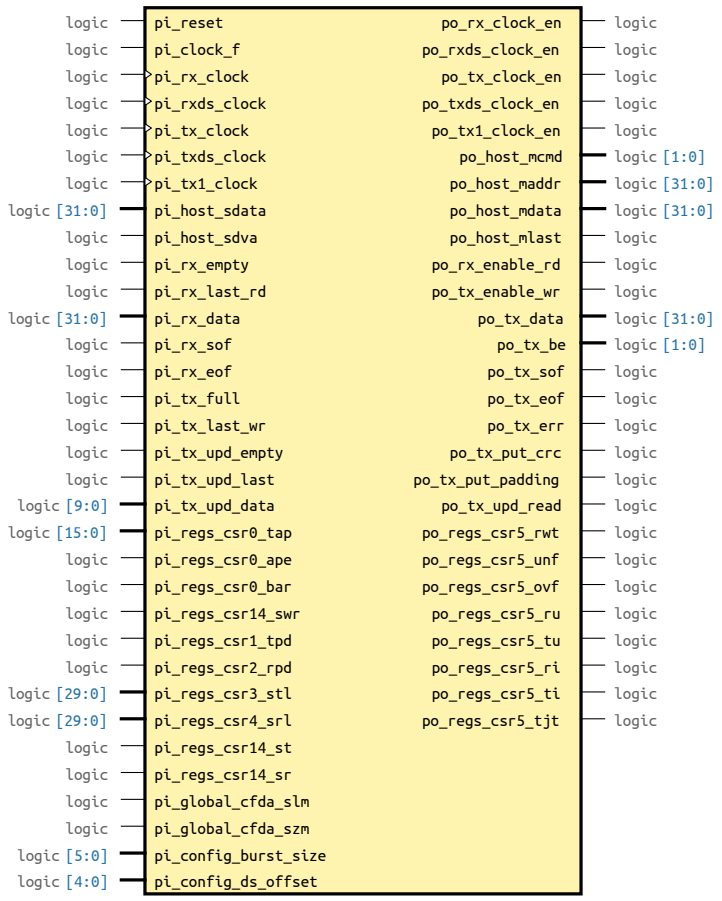

Fig. 22: Block Diagram of ip_mac_hostif_top

Table 39: Ports

Name	Type	Direction	Description
pi_reset	wire logic	input	global asynchronous reset
pi_clock_f	wire logic	input	host clock
pi_rx_clock	wire logic	input	
pi_rxds_clock	wire logic	input	
pi_tx_clock	wire logic	input	
pi_txds_clock	wire logic	input	
pi_tx1_clock	wire logic	input	
po_rx_clock_en	wire logic	output	clock enable for gated clocks
po_rxds_clock_en	wire logic	output	

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Table 39 – continued from previous page

Name	Type	Direction	Description
po_tx_clock_en	wire logic	output	
po_txds_clock_en	wire logic	output	
po_tx1_clock_en	wire logic	output	
po_host_mcmd	wire logic [1 : 0]	output	command
po_host_maddr	wire logic [31 : 0]	output	address
po_host_mdata	wire logic [31 : 0]	output	data to write
po_host_mlast	wire logic	output	last word
pi_host_sdata	wire logic [31 : 0]	input	data to read
pi_host_sdva	wire logic	input	data valid
po_rx_enable_rd	wire logic	output	rx fifo read command
pi_rx_empty	wire logic	input	rx fifo full
pi_rx_last_rd	wire logic	input	rx fifo almost full
pi_rx_data	wire logic [31 : 0]	input	rx fifo data
pi_rx_sof	wire logic	input	rx fifo eof
pi_rx_eof	wire logic	input	rx fifo eof
po_tx_enable_wr	wire logic	output	rx fifo read command
pi_tx_full	wire logic	input	rx fifo full
pi_tx_last_wr	wire logic	input	rx fifo almost full
po_tx_data	wire logic [31 : 0]	output	rx fifo data
po_tx_be	wire logic [1 : 0]	output	tx fifo data byte enable
po_tx_sof	wire logic	output	tx fifo start of frame
po_tx_eof	wire logic	output	tx fifo end of frame
po_tx_err	wire logic	output	tx fifo error
po_tx_put_crc	wire logic	output	put crc indication (valid only when sof=1)
po_tx_put_padding	wire logic	output	put padding indication (valid only when sof=1)
po_tx_upd_read	wire logic	output	

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Table 39 – continued from previous page

Name	Type	Direction	Description
pi_tx_upd_empty	wire logic	input	
pi_tx_upd_last	wire logic	input	
pi_tx_upd_data	wire logic [9 : 0]	input	
pi_regs_csr0_tap	wire logic [15 : 0]	input	tx automatic polling period CSR0[31:16]
pi_regs_csr0_ape	wire logic	input	tx auto polling enable CSR[15]
pi_regs_csr0_bar	wire logic	input	bus arbitration
pi_regs_csr14_swr	wire logic	input	software reset
pi_regs_csr1_tpd	wire logic	input	transmit poll demand
pi_regs_csr2_rpd	wire logic	input	receive poll demand
pi_regs_csr3_stl	wire logic [29 : 0]	input	transmit descriptor base address
pi_regs_csr4_srl	wire logic [29 : 0]	input	receive descriptor base address
po_regs_csr5_rwt	wire logic	output	receive watchdog timeout
po_regs_csr5_unf	wire logic	output	transmit underflow
po_regs_csr5_ovf	wire logic	output	receive overflow
po_regs_csr5_ru	wire logic	output	receive buffer unavailable
po_regs_csr5_tu	wire logic	output	transmit buffer unavailable
po_regs_csr5_ri	wire logic	output	receive interupt
po_regs_csr5_ti	wire logic	output	transmit interupt
po_regs_csr5_tjt	wire logic	output	signals Transmit jabber timeout error to the CSR5 register; this will signal to the HOST to perform a software reset to the EMAC
pi_regs_csr14_st	wire logic	input	start/stop transmit
pi_regs_csr14_sr	wire logic	input	start / stop receive
pi_global_cfda_slm	wire logic	input	sleep mode enable
pi_global_cfda_szm	wire logic	input	snooze mode enable
pi_config_burst_size	wire logic [5 : 0]	input	limit for the rx,tx burst transfers
pi_config_ds_offset	wire logic [4 : 0]	input	offset to increment the address if a descriptor

Instances

ip_emac_top : *ip_emac_top*
↪host_if : *ip_mac_hostif_top*

Submodules

ip_mac_hostif_top
↪hostif_arb : *ip_mac_hostif_arb*
↪hostif_rx : *ip_mac_hostif_rx*
↪hostif_rxds : *ip_mac_hostif_rxds*
↪hostif_tx : *ip_mac_hostif_tx*
↪hostif_txds : *ip_mac_hostif_txds*

6.23 Module ip_mac_hostif_tx

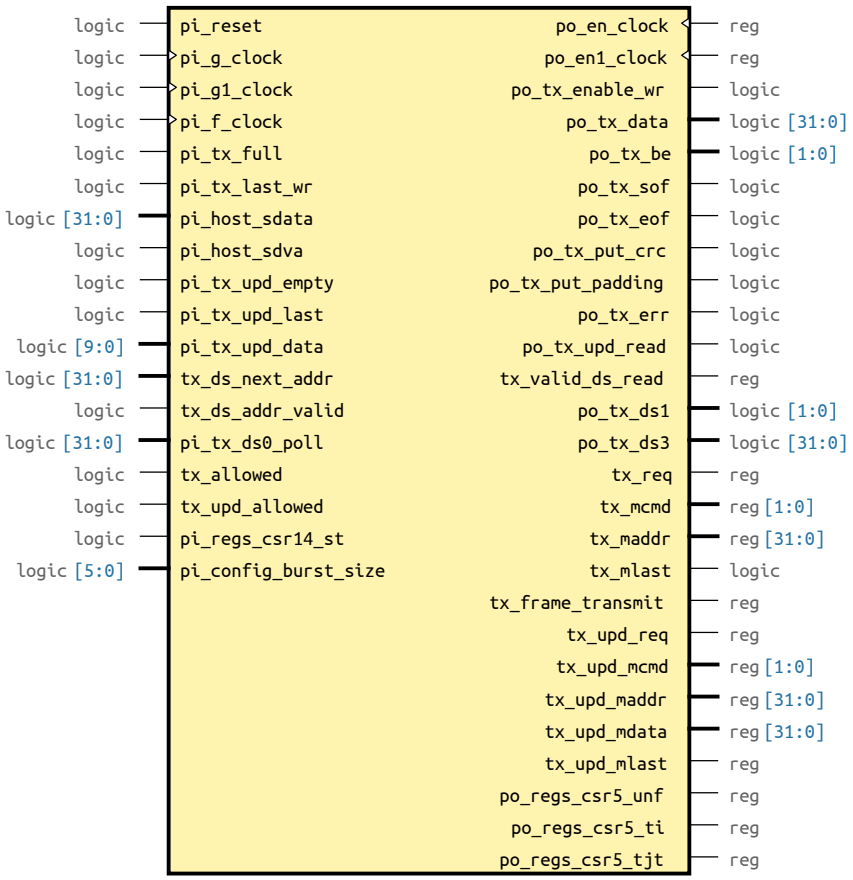

Fig. 23: Block Diagram of ip_mac_hostif_tx

Table 40: Ports

Name	Type	Direction	Description
pi_reset	wire logic	input	Global interface global asynchronous pi_reset
pi_g_clock	wire logic	input	host gated clock
pi_g1_clock	wire logic	input	host gated clock 1
pi_f_clock	wire logic	input	host free clock
po_en_clock	reg	output	enable clock condition
po_en1_clock	reg	output	enable clock condition 1
po_tx_enable_wr	wire logic	output	tx mac fifo interface rx fifo read command
pi_tx_full	wire logic	input	rx fifo full

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Table 40 – continued from previous page

Name	Type	Direction	Description
pi_tx_last_wr	wire logic	input	rx fifo almost full
po_tx_data	wire logic [31 : 0]	output	rx fifo data
po_tx_be	wire logic [1 : 0]	output	tx fifo data byte enable
po_tx_sof	wire logic	output	tx fifo start of frame
po_tx_eof	wire logic	output	tx fifo end of frame
po_tx_put_crc	wire logic	output	put crc indication (valid only when sof=1)
po_tx_put_padding	wire logic	output	put padding indication (valid only when sof=1)
po_tx_err	wire logic	output	put error indication (valid only when eof=1)
pi_host_sdata	wire logic [31 : 0]	input	host interface from host interface
pi_host_sdva	wire logic	input	from host interface
po_tx_upd_read	wire logic	output	TX update fifo interface
pi_tx_upd_empty	wire logic	input	
pi_tx_upd_last	wire logic	input	
pi_tx_upd_data	wire logic [9 : 0]	input	
tx_valid_ds_read	reg	output	ip_mac_hostif_txds to ip_mac_hostif_txds (new descriptor polling enabled)
tx_ds_next_addr	wire logic [31 : 0]	input	from ip_mac_hostif_txds (new descriptor address)
tx_ds_addr_valid	wire logic	input	from ip_mac_hostif_txds (new descriptor address valid)
pi_tx_ds0_poll	wire logic [31 : 0]	input	from ip_mac_hostif_txds (new descriptor address valid)
po_tx_ds1	wire logic [1 : 0]	output	
po_tx_ds3	wire logic [31 : 0]	output	
tx_allowed	wire logic	input	ip_mac_hostif_arb from pi_mac_hostif_-arb (tx upd req allowed)
tx_req	reg	output	request to arb from tx upd ds process
tx_mcmd	reg [1 : 0]	output	tx update ds mcmd

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Table 40 – continued from previous page

Name	Type	Direction	Description
tx_maddr	reg [31 : 0]	output	tx update ds maddr
tx_mlast	wire logic	output	tx update ds mlast
tx_frame_transmit	reg	output	to ip_mac_hostif_arb (used in arbitration process)
tx_upd_allowed	wire logic	input	from pi_mac_hostif_arb (tx upd req allowed)
tx_upd_req	reg	output	request to arb from tx upd ds process
tx_upd_mcmd	reg [1 : 0]	output	tx update ds mcmd
tx_upd_maddr	reg [31 : 0]	output	tx update ds maddr
tx_upd_mdata	reg [31 : 0]	output	tx update ds mdata
tx_upd_mlast	reg	output	tx update ds mlast
po_regs_csr5_unf	reg	output	ip_mac_regs_bank (config) transmit underflow
po_regs_csr5_ti	reg	output	transmit frame complete (to CSR5 TI)
po_regs_csr5_tjt	reg	output	transmit jabber timeout error
pi_regs_csr14_st	wire logic	input	start/stop transmit
pi_config_burst_size	wire logic [5 : 0]	input	limit for rx tx burst transfer

Always Blocks

`always@(posedge pi_g_clock or negedge pi_reset)`

state machine for tx descriptor based transfer

`always@(posedge pi_g1_clock or negedge pi_reset)`

Tx_upd_fifo holds data tx_upd_fifo_wa holds write address tx_upd_fifo_ra holds read address tx_state process write and increments tx_upd_fifo_wa tx_update_ds process read and increments tx_upd_fifo_ra

`always@(posedge pi_g1_clock or negedge pi_reset)`

This process reads from both tx_upd_fifo and tx_upd_resp_fifo, constructs TX_RDS0 and assert tx_ds_req to arbiter along with address(tx_upd_fifo) and data (tx_upd_resp_fifo)

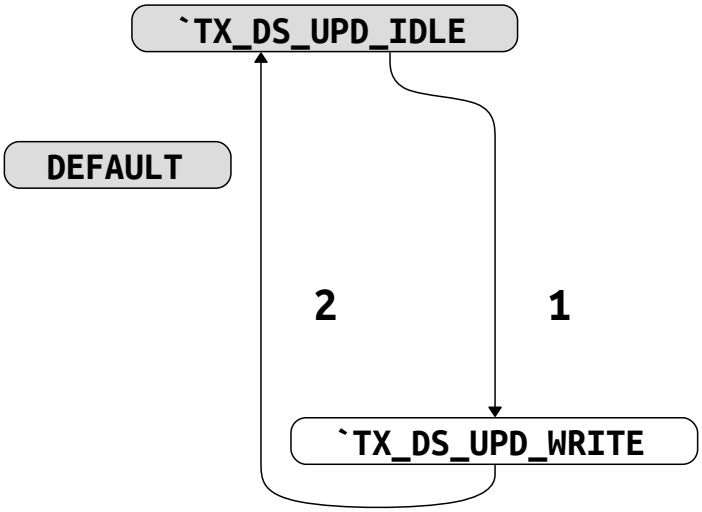

Table 41: FSM Transitions for tx_upd_state

#	Current State	Next State	Condition	Comment
1	`TX_DS_UPD_-IDLE	`TX_DS_UPD_-WRITE	[(!(~ pi_reset) && (tx_upd_req && tx_upd_allowed))]	
2	`TX_DS_UPD_-WRITE	`TX_DS_UPD_-IDLE	[(!(~ pi_reset) && (pi_host_sdva))]	

```
always@(posedge pi_f_clock or negedge pi_reset)
```

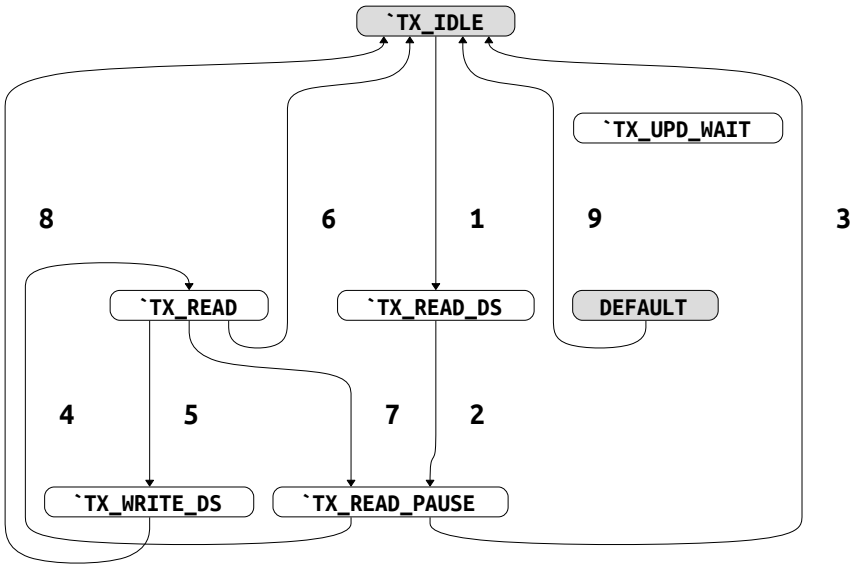

Table 42: FSM Transitions for tx_state

#	Current State	Next State	Condition	Comment
1	`TX_IDLE	`TX_READ_DS	[(!(~ pi_reset) && !(! pi_regs_csr14_st || ! tx_ds_addr_valid) && !(tx_ds_addr_valid && ! pi_tx_full && ! pi_tx_last_wr && ! tx_upd_fifo_full && ! tx_req) && (tx_allowed))]	
2	`TX_READ_DS	`TX_READ_PAUSE	[(!(~ pi_reset) && (pi_host_sdva) && !(tx_burst_cnt == 0) && !(tx_burst_cnt == 1) && (tx_burst_cnt == 2))]	
3	`TX_READ_PAUSE	`TX_IDLE	[(!(~ pi_reset) && (! tx_ds_valid))]	
4	`TX_READ_PAUSE	`TX_READ	[(!(~ pi_reset) && !(! tx_ds_valid) && !(! pi_tx_full && ! pi_tx_last_wr && ! tx_req) && (tx_allowed))]	
5	`TX_READ	`TX_WRITE_DS	[(!(~ pi_reset) && !(tx_allowed && pi_host_sdva) && (! tx_mlast && tx_word_remained && ! pi_tx_last_wr && ! pi_tx_full) && (tx_next_state == 4'b0100)), (!(~ pi_reset) && (tx_allowed && pi_host_sdva) && (tx_mlast1) && (tx_buff_cnt == tx_curr_buff_size - 1) && (tx_cur_buff || tx_ds1[24] || tx_ds1[21 : 11] == 0) && !(tx_ds1[30]) && !(tx_word_remained))]	
6	`TX_READ	`TX_IDLE	[(!(~ pi_reset) && !(tx_allowed && pi_host_sdva) && (! tx_mlast && tx_word_remained && ! pi_tx_last_wr && ! pi_tx_full) && !(tx_next_state == 4'b0100) && (tx_next_state == 4'b0000)), (!(~ pi_reset) && (tx_allowed && pi_host_sdva) && (tx_mlast1) && (tx_buff_cnt == tx_curr_buff_size - 1) && (tx_cur_buff || tx_ds1[24] || tx_ds1[21 : 11] == 0) && (tx_ds1[30]) && !(tx_word_remained))]	
7	`TX_READ	`TX_READ_PAUSE	[(!(~ pi_reset) && !(tx_allowed && pi_host_sdva) && (! tx_mlast && tx_word_remained && ! pi_tx_last_wr && ! pi_tx_full) && !(tx_next_state == 4'b0100) && !(tx_next_state == 4'b0000)), (!(~ pi_reset) && (tx_allowed && pi_host_sdva) && (tx_mlast1) && !(tx_buff_cnt == tx_curr_buff_size - 1) && (tx_burst_cnt == pi_config_burst_size - 1) && !(tx_word_remained)), (!(~ pi_reset) && (tx_allowed && pi_host_sdva) && (tx_mlast1) && (tx_buff_cnt == tx_curr_buff_size - 1) && !(tx_cur_buff || tx_ds1[24] || tx_ds1[21 : 11] == 0) && !(tx_word_remained))]	

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Table 42 – continued from previous page

#	Current State	Next State	Condition	Comment
8	`TX_WRITE_DS	`TX_IDLE	[(!(~ pi_reset) && (tx_allowed && pi_host_sdva))]	
9	default	`TX_IDLE	[!(~ pi_reset)]	Illegal state

Instances

ip_emac_top : *ip_emac_top*
↪host_if : *ip_mac_hostif_top*
↪hostif_tx : *ip_mac_hostif_tx*

6.24 Module ip_mac_hostif_txds

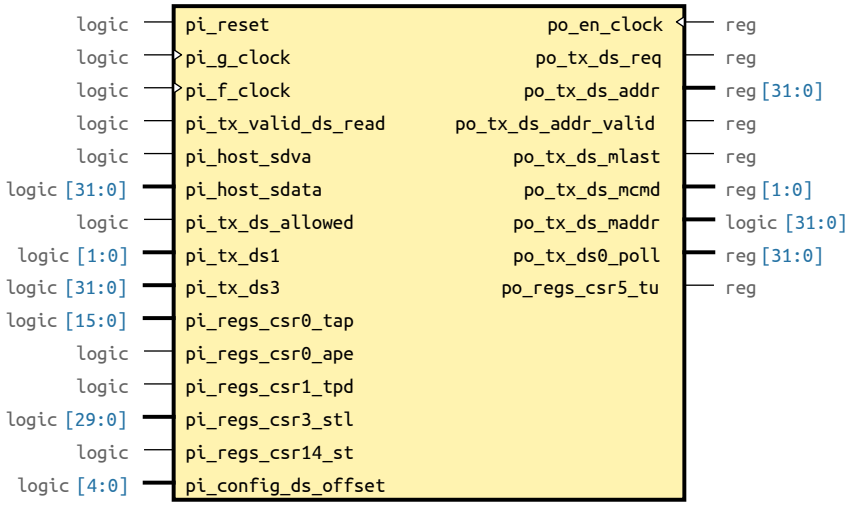

Fig. 24: Block Diagram of ip_mac_hostif_txds

Table 43: Ports

Name	Type	Direction	Description
pi_reset	wire logic	input	Global interface global asynchronous pi_reset
pi_g_clock	wire logic	input	host pi_g_clock
pi_f_clock	wire logic	input	host pi_g_clock
po_en_clock	reg	output	enable clock condition
po_tx_ds_req	reg	output	output
po_tx_ds_addr	reg [31 : 0]	output	output , mapped to old tx_ds_next_addr
po_tx_ds_addr_valid	reg	output	output
po_tx_ds_mlast	reg	output	output
po_tx_ds_mcmd	reg [1 : 0]	output	output
po_tx_ds_maddr	wire logic [31 : 0]	output	output
pi_tx_valid_ds_read	wire logic	input	from pi_mac_hostif_tx (signals that new ds polling is enabled)
pi_host_sdva	wire logic	input	
pi_host_sdata	wire logic [31 : 0]	input	
pi_tx_ds_allowed	wire logic	input	pi_host_serr, //from host interface

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Table 43 – continued from previous page

Name	Type	Direction	Description
po_tx_ds0_poll	reg [31 : 0]	output	
pi_tx_ds1	wire logic [1 : 0]	input	mapped to tx pi_tx_ds1[25:24]
pi_tx_ds3	wire logic [31 : 0]	input	
pi_regs_csr0_tap	wire logic [15 : 0]	input	Registers bank interface tx automatic polling period CSR0[31:16]
pi_regs_csr0_ape	wire logic	input	tx auto polling enable CSR[15]
pi_regs_csr1_tpd	wire logic	input	transmit poll demand
pi_regs_csr3_stl	wire logic [29 : 0]	input	transmit descriptor base address
po_regs_csr5_tu	reg	output	transmit buffer unavailable
pi_regs_csr14_st	wire logic	input	start/stop transmit
pi_config_ds_offset	wire logic [4 : 0]	input	offset to increment the address if a descriptor

Always Blocks

always@(posedge pi_g_clock or negedge pi_reset)

Manages the next descriptor aquire

always@(posedge pi_f_clock or negedge pi_reset)

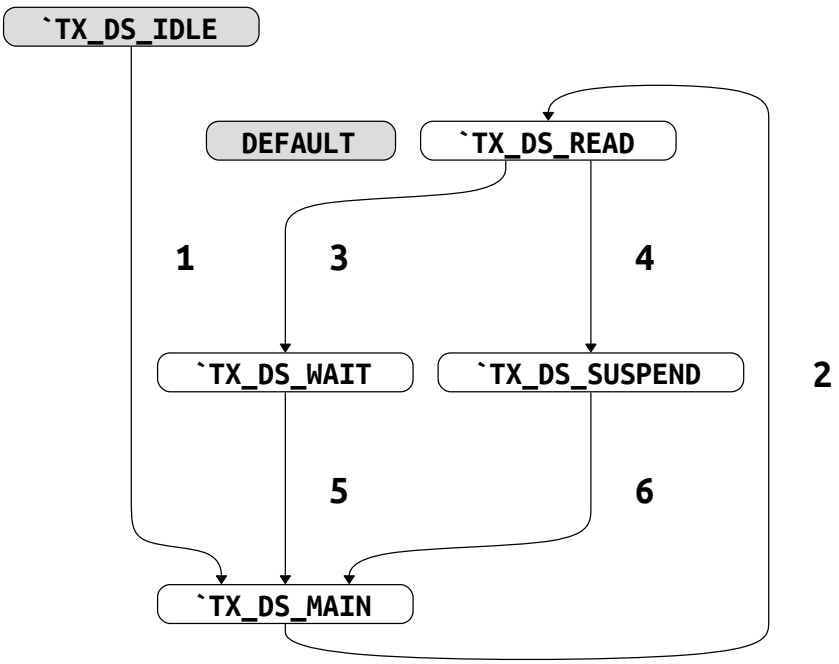

Table 44: FSM Transitions for tx_ds_state

#	Current State	Next State	Condition	Comment
1	`TX_DS_IDLE	`TX_DS_MAIN	[(!(~ pi_reset) && !(! pi_regs_csr14_st))]	
2	`TX_DS_MAIN	`TX_DS_READ	[(!(~ pi_reset) && (pi_tx_ds_allowed))]	
3	`TX_DS_READ	`TX_DS_WAIT	[(!(~ pi_reset) && (pi_host_sdva) && (pi_host_sdata[31]))]	
4	`TX_DS_READ	`TX_DS_SUSPEND	[(!(~ pi_reset) && (pi_host_sdva) && !(pi_host_sdata[31]))]	
5	`TX_DS_WAIT	`TX_DS_MAIN	[(!(~ pi_reset) && (pi_tx_valid_ds_read))]	
6	`TX_DS_SUSPEND	`TX_DS_MAIN	[(!(~ pi_reset) && (pi_regs_csr0_ape && tx_ds_poll_cnt == pi_regs_csr0_tap || pi_regs_csr1_tpd))]	

Instances

ip_emac_top : *ip_emac_top*
↪host_if : *ip_mac_hostif_top*
↪hostif_txds : *ip_mac_hostif_txds*

6.25 Module ip_mac_mdio_g

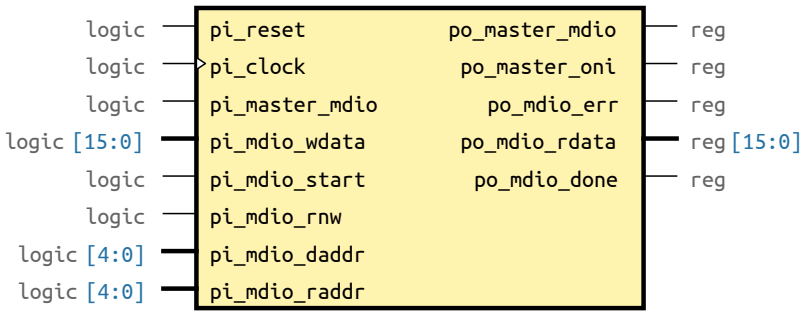

Fig. 25: Block Diagram of ip_mac_mdio_g

Overview

The EMAC has a master management interface, which is used to access the PHY configuration registers. Depending on the configuration, the EMAC will either read the values from the PHY registers (auto-configuration mode) or set the values according to the programmed values (programming mode). The MDIO (po_master_mdio/pi_master_mdio) and MDC (po_master_mdc) ports are used to serially write and read management interface registers. A 2.5 MHz clock waveform must be provided to the MDC port on this interface.

Every management read/write instruction frame contains the following fields:

- PRE, Preamble - The EMAC management interface generates a full 32-bit preamble
- ST, Start of Frame (A "01" pattern indicates the start of frame)
- OP, Operation Code - A read instruction is indicated by "01", while a write instruction is indicated by "10"
- DEVAD, Device Address - A five-bit device address follows the opcode, with the most significant bit transmitted first.
- REGAD, Register Address - A five-bit register address follows the DEVAD field, with the most significant bit transmitted first. This field is used to access the management registers of the PHY.
- TA, Turnaround - The next two bit times are used to avoid contention on the MDIO port during a read transaction. For a read transaction, the PHY device and the system MDIO should be in tri-state for the first cycle of turnaround. The PHY device drives zero during the second cycle of the turnaround. For write transactions, the EMAC should drive 1 during the first cycle of the turnaround and zero during the second cycle.
- Data - The last 16 bits of the frame are the actual data bits. For a write operation, these bits are sent to the PHY device. For a read operation, the PHY device drives these bits. In both cases, the most significant bit is transmitted first.
- Idle - This indicates a high-impedance state of the MDIO line. The default state of the MDIO signal is high impedance with a pull-up resistor.

Table 45: Ports

Name	Type	Direction	Description
pi_reset	wire logic	input	Global reset (asynchronous reset)
pi_clock	wire logic	input	Master MDIO reference clock
pi_master_mdio	wire logic	input	MDIO interface Master MDIO data input line (tri-state buffer outside of the module)

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Table 45 – continued from previous page

Name	Type	Direction	Description
po_master_mdio	reg	output	Master MDIO data output line (tri-state buffer outside of the module)
po_master_oni	reg	output	Master MDIO direction tri-state buffer control (1 - Output, 0 - Input)
po_mdio_err	reg	output	Configuration interface (HOST clock domain) Indicates that a read from MDIO interface is invalid and the
pi_mdio_wdata	wire logic [15 : 0]	input	operation should be retried. This is indicated during a read turn-around cycle when the MDIO slave does not drive the MDIO signal to the low state. MDIO write data
po_mdio_rdata	reg [15 : 0]	output	MDIO read data
pi_mdio_start	wire logic	input	Setting this bit initiates an MDIO read/write operation. Start indication
po_mdio_done	reg	output	should remain asserted till the transaction complete. (asynchronous) MDIO transaction complete
pi_mdio_rnw	wire logic	input	This bit indicates the direction of the MDIO operation type:
pi_mdio_daddr	wire logic [4 : 0]	input	0 - MDIO Write operation, 1 - MDIO read operation This field is used to specify the device address to be accessed.
pi_mdio_raddr	wire logic [4 : 0]	input	This field is used to specify the register address to be accessed.

Always Blocks

`always@(posedge pi_clock or negedge pi_reset)`

MDIO State Machine

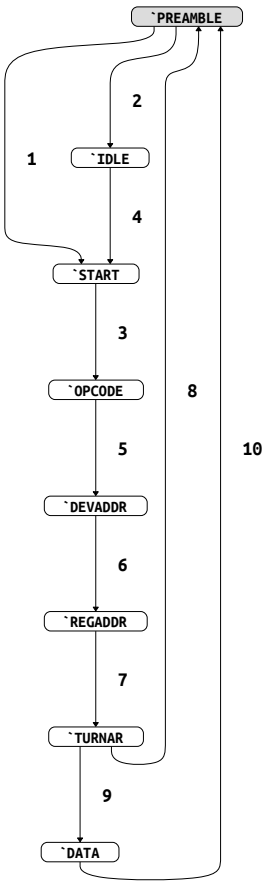

Table 46: FSM Transitions for mdio_state

#	Current State	Next State	Condition	Comment
1	`PREAMBLE	`START	[(!(~ pi_reset) && (counter == 5'd0 && mdio_start == 1'b1))]	
2	`PREAMBLE	`IDLE	[(!(~ pi_reset) && (counter == 5'd0))]	
3	`START	`OPCODE	[(!(~ pi_reset) && (counter == 5'd0))]	
4	`IDLE	`START	[(!(~ pi_reset) && (mdio_start == 1'b1))]	
5	`OPCODE	`DEVADDR	[(!(~ pi_reset) && (counter == 5'd0))]	
6	`DEVADDR	`REGADDR	[(!(~ pi_reset) && (counter == 5'd31))]	
7	`REGADDR	`TURNAR	[(!(~ pi_reset) && (counter == 5'd31))]	
8	`TURNAR	`PREAMBLE	[(!(~ pi_reset) && (counter == 5'd0 && pi_master_mdio != 1'b0 && pi_-mdio_rnw == 1'b1))]	
9	`TURNAR	`DATA	[(!(~ pi_reset) && !(counter == 5'd0 && pi_master_mdio != 1'b0 && pi_-mdio_rnw == 1'b1) && (counter == 5'd0))]	
10	`DATA	`PREAMBLE	[(!(~ pi_reset) && (counter == 5'd31))]	

```
always@(posedge pi_clock or negedge pi_reset)
```

HOST to MDIO clock domain synchronization

Instances

ip_emac_top : *ip_emac_top*
↪mac_top : *ip_mac_top_g*
↪mac_mdio : *ip_mac_mdio_g*

6.26 Module ip_mac_regs_bank

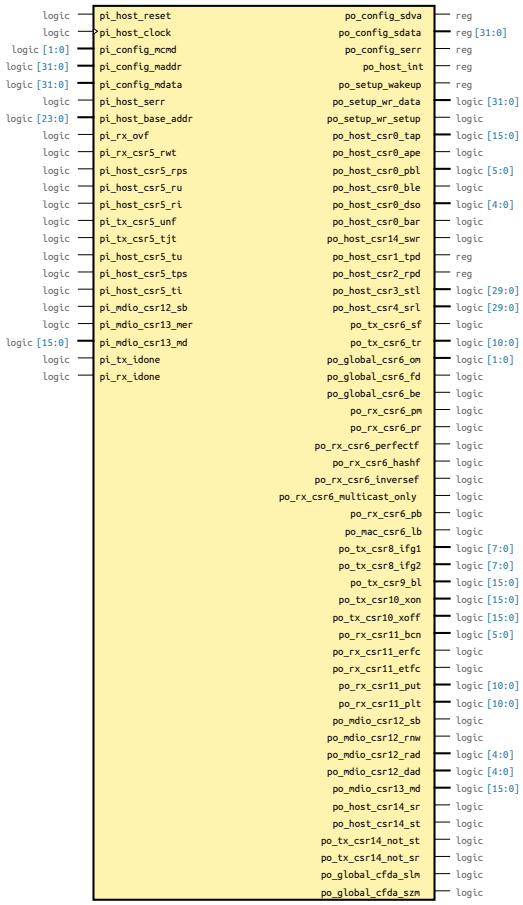

Fig. 26: Block Diagram of ip_mac_regs_bank

Table 47: Ports

Name	Type	Direction	Description
pi_host_reset	wire logic	input	general interface host domain reset
pi_host_clock	wire logic	input	host domain clock
pi_config_mcmd	wire logic [1 : 0]	input	host access interface
pi_config_maddr	wire logic [31 : 0]	input	
pi_config_mdata	wire logic [31 : 0]	input	
po_config_sdva	reg	output	pi_config_mlast,
po_config_sdata	reg [31 : 0]	output	
po_config_serr	reg	output	
pi_host_serr	wire logic	input	failure on host data interface

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Table 47 – continued from previous page

Name	Type	Direction	Description
pi_host_base_addr	wire logic [23 : 0]	input	internal space base address
po_host_int	reg	output	general interrupt to the host
po_setup_wakeup	reg	output	setup interface
po_setup_wr_data	wire logic [31 : 0]	output	
po_setup_wr_setup	wire logic	output	
po_host_csr0_tap	wire logic [15 : 0]	output	host domain register outputs & inputs
po_host_csr0_ape	wire logic	output	
po_host_csr0_pbl	wire logic [5 : 0]	output	
po_host_csr0_ble	wire logic	output	
po_host_csr0_dso	wire logic [4 : 0]	output	
po_host_csr0_bar	wire logic	output	
po_host_csr14_swr	wire logic	output	
po_host_csr1_tpd	reg	output	transmit poll demand
po_host_csr2_rpd	reg	output	receive poll demand
po_host_csr3_stl	wire logic [29 : 0]	output	transmit descriptor base address
po_host_csr4_srl	wire logic [29 : 0]	output	receive descriptor base address
pi_rx_ovf	wire logic	input	reveive overflow (from HOST If Rx statistic compilation)
pi_rx_csr5_rwt	wire logic	input	pi_host_csr5_ts, //transmit process state pi_host_csr5_rs, //receive process state receive watchdog timeout(16k limit)
pi_host_csr5_rps	wire logic	input	receive process stopped
pi_host_csr5_ru	wire logic	input	receive buffer unavailable
pi_host_csr5_ri	wire logic	input	receive interupt
pi_tx_csr5_unf	wire logic	input	transmit underflow (from HOST If Tx statistic compilation)
pi_tx_csr5_tjt	wire logic	input	transmit jabber time-out
pi_host_csr5_tu	wire logic	input	transmit buffer unavailable

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Table 47 – continued from previous page

Name	Type	Direction	Description
pi_host_csr5_tps	wire logic	input	transmit process stopped
pi_host_csr5_ti	wire logic	input	transmit interrupt
po_tx_csr6_sf	wire logic	output	transmission store and forward OR transmit when threshold csr6[24:14] reached
po_tx_csr6_tr	wire logic [10 : 0]	output	transmission threshold
po_global_csr6_om	wire logic [1 : 0]	output	global operating mode (10/100/1G)
po_global_csr6_fd	wire logic	output	full-duplex mode enable
po_global_csr6_be	wire logic	output	burst enable (when 1G mode selected)
po_rx_csr6_pm	wire logic	output	receive pass all multicast enable
po_rx_csr6_pr	wire logic	output	receive promiscuous mode enable
po_rx_csr6_perfectf	wire logic	output	perfect filtering
po_rx_csr6_hashf	wire logic	output	hash filtering
po_rx_csr6_inversef	wire logic	output	inverse filtering
po_rx_csr6_multicast_-only	wire logic	output	imperfect filtering
po_rx_csr6_pb	wire logic	output	receive pass bad frames
po_mac_csr6_lb	wire logic	output	loopback mode enable
po_tx_csr8_ifg1	wire logic [7 : 0]	output	pi_rx_csr8_mfc_inc, // missed frame counter increment command IFG1
po_tx_csr8_ifg2	wire logic [7 : 0]	output	IFG2
po_tx_csr9_bl	wire logic [15 : 0]	output	burst length
po_tx_csr10_xon	wire logic [15 : 0]	output	tx pause xon
po_tx_csr10_xoff	wire logic [15 : 0]	output	tx pause xoff
po_rx_csr11_bcn	wire logic [5 : 0]	output	receive backpressure collision number
po_rx_csr11_erfc	wire logic	output	receive enable flow control
po_rx_csr11_etfc	wire logic	output	transmit enable flow control
po_rx_csr11_put	wire logic [10 : 0]	output	pause upper threshold
po_rx_csr11_plt	wire logic [10 : 0]	output	pause lower threshold

continues on next page

Table 47 – continued from previous page

Name	Type	Direction	Description
po_mdio_csr12_sb	wire logic	output	MDIO start
pi_mdio_csr12_sb	wire logic	input	mdio busy
po_mdio_csr12_rnw	wire logic	output	MDIO r/w
po_mdio_csr12_rad	wire logic [4 : 0]	output	MDIO register address
po_mdio_csr12_dad	wire logic [4 : 0]	output	MDIO device address
pi_mdio_csr13_mer	wire logic	input	mdio error
po_mdio_csr13_md	wire logic [15 : 0]	output	MDIO write data to MDIO if
pi_mdio_csr13_md	wire logic [15 : 0]	input	MDIO read data from MDIO if
po_host_csr14_sr	wire logic	output	start / stop receive
po_host_csr14_st	wire logic	output	start / stop transmit
po_tx_csr14_not_st	wire logic	output	tx stop transmit
po_tx_csr14_not_sr	wire logic	output	rx stop receive
pi_tx_idone	wire logic	input	MAC tx initialization done
pi_rx_idone	wire logic	input	MAC rx initialization done
po_global_cfda_slm	wire logic	output	sleep mode enable
po_global_cfda_szm	wire logic	output	snooze mode enable

Always Blocks

`always@(negedge pi_host_reset or posedge pi_host_clock)`

R/W registers

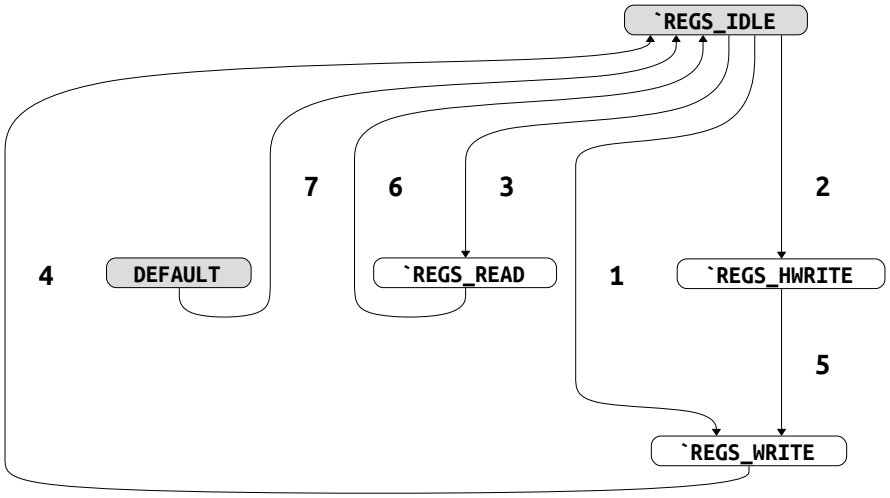
`REGS_IDLE
7
6
3
2
4
DEFAULT
`REGS_READ
1
`REGS_HWRITE
5
`REGS_WRITE

Table 48: FSM Transitions for config_state

#	Current State	Next State	Condition	Comment
1	`REGS_IDLE	`REGS_WRITE	[(!(~ pi_host_reset) && (device_selected) && (pi_config_mcmd == 2'b01) && (rw_addr == 7'h00)), (!(~ pi_host_reset) && (device_selected) && (pi_config_mcmd == 2'b01) && (rw_addr == 7'h04)), (!(~ pi_host_reset) && (device_selected) && (pi_config_mcmd == 2'b01) && (rw_addr == 7'h08)), (!(~ pi_host_reset) && (device_selected) && (pi_config_mcmd == 2'b01) && (rw_addr == 7'h0c)), (!(~ pi_host_reset) && (device_selected) && (pi_config_mcmd == 2'b01) && (rw_addr == 7'h10)), (!(~ pi_host_reset) && (device_selected) && (pi_config_mcmd == 2'b01) && (rw_addr == 7'h14)), (!(~ pi_host_reset) && (device_selected) && (pi_config_mcmd == 2'b01) && (rw_addr == 7'h18)), (!(~ pi_host_reset) && (device_selected) && (pi_config_mcmd == 2'b01) && (rw_addr == 7'h1c)), (!(~ pi_host_reset) && (device_selected) && (pi_config_mcmd == 2'b01) && (rw_addr == 7'h20)), (!(~ pi_host_reset) && (device_selected) && (pi_config_mcmd == 2'b01) && (rw_addr == 7'h24)), (!(~ pi_host_reset) && (device_selected) && (pi_config_mcmd == 2'b01) && (rw_addr == 7'h28)), (!(~ pi_host_reset) && (device_selected) && (pi_config_mcmd == 2'b01) && (rw_addr == 7'h2c)), (!(~ pi_host_reset) && (device_selected) && (pi_config_mcmd == 2'b01) && (rw_addr == 7'h30)), (!(~ pi_host_reset) && (device_selected) && (pi_config_mcmd == 2'b01) && (rw_addr == 7'h34)), (!(~ pi_host_reset) && (device_selected) && (pi_config_mcmd == 2'b01) && (rw_addr == 7'h38)), (!(~ pi_host_reset) && (device_selected) && (pi_config_mcmd == 2'b01) && (rw_addr == 7'h3c)), (!(~ pi_host_reset) && (device_selected) && (pi_config_mcmd == 2'b01) && (rw_addr == 7'h40)), (!(~ pi_host_reset) && (device_selected) && (pi_config_mcmd == 2'b01) && (rw_addr == 7'h44))]	

continues on next page

Table 48 – continued from previous page

#	Current State	Next State	Condition	Comment
2	`REGS_IDLE	`REGS_HWRITE	[(!(~ pi_host_reset) && (device_selected) && (pi_config_mcmd == 2'b01) && (rw_addr == 7'h48))]	
3	`REGS_IDLE	`REGS_READ	[(!(~ pi_host_reset) && (device_selected) && !(pi_config_mcmd == 2'b01) && (pi_config_mcmd == 2'b10))]	
4	`REGS_WRITE	`REGS_IDLE	[!(~ pi_host_reset)]	
5	`REGS_HWRITE	`REGS_WRITE	[(!(~ pi_host_reset) && (hash_cnt == 1))]	
6	`REGS_READ	`REGS_IDLE	[!(~ pi_host_reset)]	
7	default	`REGS_IDLE	[!(~ pi_host_reset)]	

Instances

ip_emac_top : *ip_emac_top*
↪regs_bank : *ip_mac_regs_bank*

6.27 Module ip_mac_rx_fifo_g

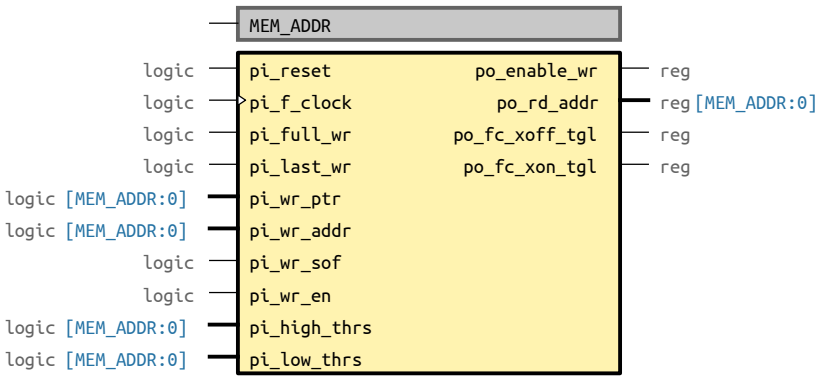

Fig. 27: Block Diagram of ip_mac_rx_fifo_g

Overview

The EMAC Receive FIFO Control module is responsible to generate all the control signals necessary to transfer the data form the EMAC Receive Memory module to the EMAC Asynchronous FIFO module. The EMAC Receive FIFO Control module provides the memory write memory pointer and the write address, used by the EMAC Receive module in order to calculate if the memory is ready (actual frame transmission begins after the internal Receive memory had reached either a programmable threshold or after a full frame is contained in the memory). The write address is updated (takes the write pointer value) whenever the memory contains enough data for Receive. The pointer update is made when the number of words of the frame exceeds a programmed threshold value or the entire frame is in the memory.

Table 49: Parameters

Name	Default	Description
MEM_ADDR	6	Transmit memory address width (9 -> 512 locations, 10->1024)

Table 50: Ports

Name	Type	Direction	Description
pi_reset	wire logic	input	Global Hardware/Software reset (active low)
pi_f_clock	wire logic	input	Receive GMII/MII 125/25/2.5 MHz clock (from Clock Manager)
pi_full_wr	wire logic	input	Signals from/to Asynchronous FIFO Asynchronous FIFO full (no write can be performed)
pi_last_wr	wire logic	input	Asynchronous FIFO last valid location
po_enable_wr	reg	output	Asynchronous FIFO write enable

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Table 50 – continued from previous page

Name	Type	Direction	Description
pi_wr_ptr	wire logic [*MEM_ADDR* : 0]	input	Signals from MAC State Machine Used by RX FIFO to compute the memory state (full/empty/ready)
pi_wr_addr	wire logic [*MEM_ADDR* : 0]	input	Write address (memory write address)
po_rd_addr	reg [*MEM_ADDR* : 0]	output	Used by EMAC Receive State to see the momory state (full/empty/ready)
pi_wr_sof	wire logic	input	Memory SOF and write enable (use for fc toggle function) Start of frame indication (resend a new FC packet since
pi_wr_en	wire logic	input	a new frame was received during pause period, a previously FC was send) FIFO write enable (valid start of frame)
pi_high_thrs	wire logic [*MEM_ADDR* : 0]	input	Flow control From configuration FC high threshold
pi_low_thrs	wire logic [*MEM_ADDR* : 0]	input	From configuration FC low threshold
po_fc_xoff_tgl	reg	output	(to TX EMAC) insert XOFF flow control information
po_fc_xon_tgl	reg	output	(to TX EMAC) insert XON flow control information

Always Blocks

`always@(posedge pi_f_clock or negedge pi_reset)`

Low/High Threshold Assignment

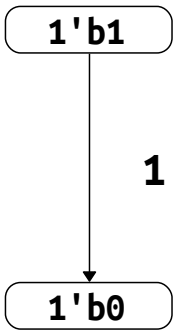

Table 51: FSM Transitions for high_low_en

#	Current State	Next State	Condition	Comment
1	1'b1	1'b0	[(!(~ pi_reset) && !(pi_high_thrs < fifo_level && pi_wr_en == 1'b1 && pi_wr_sof == 1'b1))]	

always@(posedge pi_f_clock or negedge pi_reset)

Number of full locations

always@(po_rd_addr or pi_wr_ptr or po_enable_wr or read_inc)

Assign FIFO empty (move memory address when empty)

always@(posedge pi_f_clock or negedge pi_reset)

Write Enable & Address/Pointer Update Process

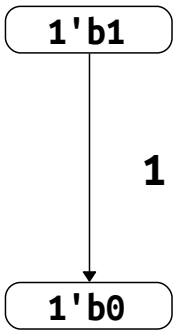

Table 52: FSM Transitions for po_enable_wr

#	Current State	Next State	Condition	Comment
1	1'b1	1'b0	[(!(~ pi_reset) && !(valid_data == 1'b0) && !(pi_full_wr == 1'b1))]	

Instances

ip_emac_top : *ip_emac_top*
↪mac_top : *ip_mac_top_g*
↪mac_rx_top : *ip_mac_rx_top_g*
↪rx_fifo : *ip_mac_rx_fifo_g* #(.MEM_ADDR(10))

6.28 Module ip_mac_rx_gmii_g

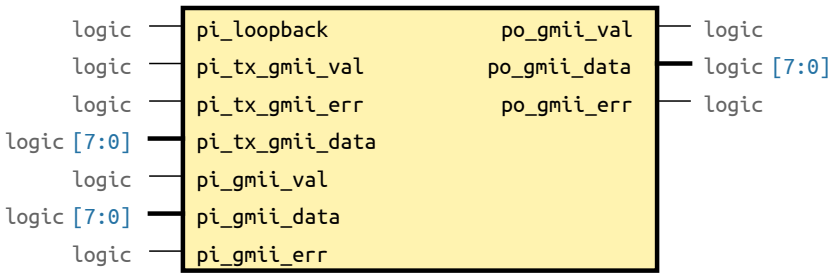

Fig. 28: Block Diagram of ip_mac_rx_gmii_g

Overview

The EMAC Receive MII/GMII module is responsible to multiplex the MII input interface (nibble oriented) signals coming from physical layer into GMII format when 10/100 Mbps operating mode is selected or to pass the GMII signal to the EMAC Receive State Machine when operating speed above 100 Mbps.

The EMAC Receive MII/GMII module it also checks for invalid Ethernet MAC frames by checking for proper byte-boundary alignment of the end of the frame. The block is responsible to generate the alignment error indication when frame length is not an integer number of bytes.

The module is also responsible for the internal loop-back operation, when the EMAC operates in loop-back mode. The EMAC Clock Manager module is responsible to switch between the input receive clock and transmit clock for loop-back operation.

Table 53: Ports

Name	Type	Direction	Description
pi_loopback	wire logic	input	Loopback mode select
pi_tx_gmii_val	wire logic	input	Loopback Info Loopback MII/GMII data valid indication (from TX)
pi_tx_gmii_err	wire logic	input	Loopback MII/GMII error indication (from TX)
pi_tx_gmii_data	wire logic [7 : 0]	input	Loopback MII/GMII data (MII data is pi_emac_rx_data[3:0]) (from TX)
pi_gmii_val	wire logic	input	gmii Data Valid, Data Input Signals and Alignment Error Receive MII/GMII data valid indication (from PHY)
pi_gmii_data	wire logic [7 : 0]	input	Receive MII/GMII error indication (from PHY)
pi_gmii_err	wire logic	input	Receive MII/GMII data (MII data is pi_emac_rx_data[3:0]) (from PHY)

continues on next page

Table 53 – continued from previous page

Name	Type	Direction	Description
po_gmii_val	wire logic	output	GMII Data Valid, Data Input Signals and Alignment Error Receive MII/GMII data valid indication (to RX state)
po_gmii_data	wire logic [7 : 0]	output	Receive MII/GMII error indication (to RX state)
po_gmii_err	wire logic	output	Receive MII/GMII data (MII data is pi_emac_rx_data[3:0]) (to RX state)

Instances

ip_emac_top : *ip_emac_top*
↪mac_top : *ip_mac_top_g*
↪mac_rx_top : *ip_mac_rx_top_g*
↪rx_gmii : *ip_mac_rx_gmii_g*

6.29 Module ip_mac_rx_hash_g

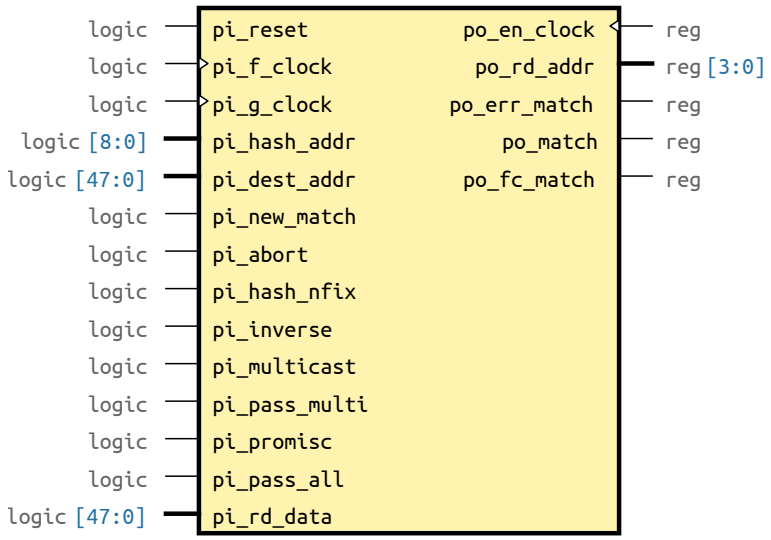

Fig. 29: Block Diagram of ip_mac_rx_hash_g

Overview

Imperfect filtering The EMAC Receive Hash/Exact Mach module is responsible for received frame filtering. For any incoming multicast frame, the EMAC applies the standard Ethernet cyclic redundancy check (CRC) function to the first 6 bytes that contain the destination address, then, if the hash filtering type is selected, the EMAC Receive Hash/Exact Mach module uses the most significant 9 bits (for a 512 bit hash table) of the result as a bit index into a table. If the indexed bit is set, the multicast frame is accepted. If the bit is cleared, the multicast frame is rejected. This filtering mode is called imperfect because frames not addressed to this station may slip through, but it still decreases the number of frames that the host can receive.

Perfect filtering The EMAC interprets a setup frame buffer in perfect filtering mode if the configuration bits are set accordingly. The EMAC can store 16 (programmable) destination addresses (full 48-bit Ethernet addresses). The EMAC compares the addresses of any incoming frame to these addresses, and also tests the status of the inverse filtering. It rejects addresses that: - Do not match if inverse filtering - Match if perfect filtering is set The setup frame must supply all 16 (programmable) addresses. Any mix of physical and multicast addresses can be used. Unused addresses should duplicate one of the valid addresses.

Table 54: Ports

Name	Type	Direction	Description
pi_reset	wire logic	input	Global Software/Hardware Reset (receive clock domain)
pi_f_clock	wire logic	input	Free Receive GMII/MII 125/25/2.5 MHz clock (from Clock Manager)
pi_g_clock	wire logic	input	Gated Receive GMII/MII 125/25/2.5 MHz clock (from Clock Manager)

continues on next page

Table 54 – continued from previous page

Name	Type	Direction	Description
po_en_clock	reg	output	Receive GMII/MII 125/25/2.5 MHz clock gated clock enable
pi_hash_addr	wire logic [8 : 0]	input	From Receive EMAC Hash table index (9-MSB of CRC calculation over 48-bit destination address)
pi_dest_addr	wire logic [47 : 0]	input	Exact match (destination address of the frame)
pi_new_match	wire logic	input	Start a new search (match address, or hash filtering, toggle signal when new match should be prformed)
pi_abort	wire logic	input	Abort search (due to errors)
pi_hash_nfix	wire logic	input	Configuration Hash filtering + 1 Address match / 16 Address match
pi_inverse	wire logic	input	Inverse match
pi_multicast	wire logic	input	When asserted the imperfect filtering refers only for multicast addressees
pi_pass_multi	wire logic	input	Pass all multicast addresses
pi_promisc	wire logic	input	Promiscuos Mode (no DA filter)
pi_pass_all	wire logic	input	Pass all frames (bad or good)
pi_rd_data	wire logic [47 : 0]	input	Hash Table Memory access Memory (hash table) read data
po_rd_addr	reg [3 : 0]	output	Memory (hash table) read address
po_err_match	reg	output	Match Address Hit Address match output error
po_match	reg	output	Address match output
po_fc_match	reg	output	Address match output (control frame address)

Always Blocks

`always@(posedge pi_g_clock or negedge pi_reset)`

Filtering FSM

`always@(posedge pi_g_clock or negedge pi_reset)`

Assign New Match Process

`always@(posedge pi_f_clock or negedge pi_reset)`

Gated Clock Enable

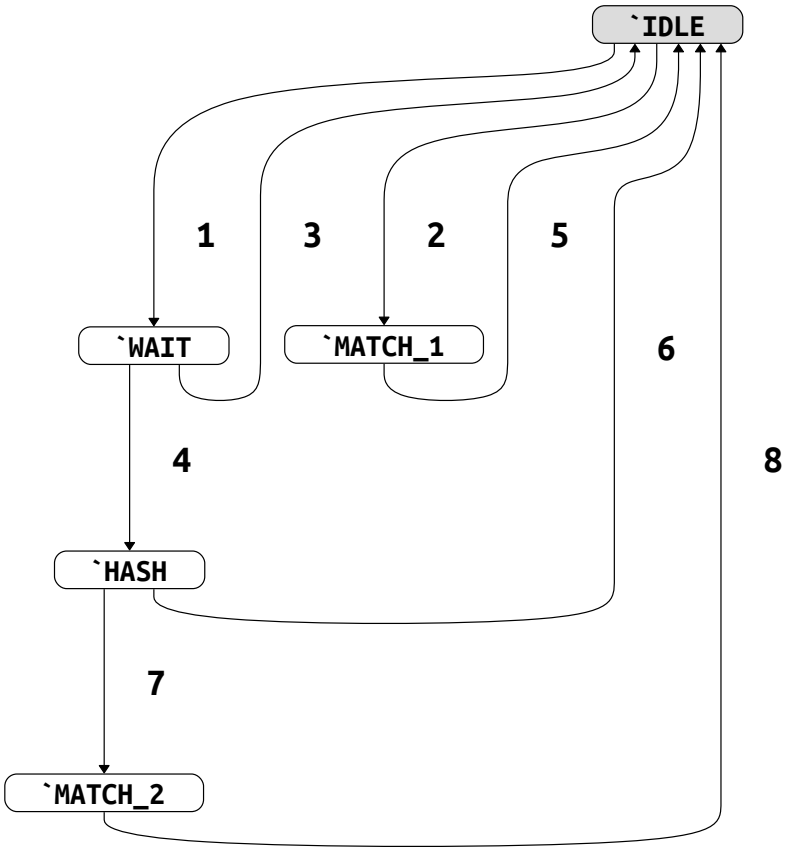

Table 55: FSM Transitions for fsm_hash_st

#	Current State	Next State	Condition	Comment
1	`IDLE	`WAIT	[(!(~ pi_reset) && !(pi_abort == 1'b0 && new_match == 1'b1 && pi_dest_addr == 48'h0180C2000001) && !(pi_abort == 1'b0 && new_match == 1'b1 && pi_promisc == 1'b1 || pi_pass_all == 1'b1) && !(pi_abort == 1'b0 && new_match == 1'b1 && pi_pass_multi == 1'b1 && pi_dest_addr[40] == 1'b1) && (pi_abort == 1'b0 && new_match == 1'b1 && pi_hash_nfix == 1'b1))]	

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Table 55 – continued from previous page

#	Current State	Next State	Condition	Comment
2	`IDLE	`MATCH_1	[(!(~ pi_reset) && !(pi_abort == 1'b0 && new_match == 1'b1 && pi_dest_addr == 48'h0180C2000001) && !(pi_abort == 1'b0 && new_match == 1'b1 && pi_promisc == 1'b1 || pi_pass_all == 1'b1) && !(pi_abort == 1'b0 && new_match == 1'b1 && pi_pass_multi == 1'b1 && pi_dest_addr[40] == 1'b1) && !(pi_abort == 1'b0 && new_match == 1'b1 && pi_hash_nfix == 1'b1) && (pi_abort == 1'b0 && new_match == 1'b1))]	
3	`WAIT	`IDLE	[(!(~ pi_reset) && (pi_abort == 1'b1))]	
4	`WAIT	`HASH	[(!(~ pi_reset) && !(pi_abort == 1'b1))]	
5	`MATCH_1	`IDLE	[(!(~ pi_reset) && (pi_abort == 1'b1)), (!(~ pi_reset) && !(pi_abort == 1'b1) && (pi_rd_data == pi_dest_addr)), (!(~ pi_reset) && !(pi_abort == 1'b1) && !(pi_rd_data == pi_dest_addr) && (po_rd_addr == 4'h0))]	
6	`HASH	`IDLE	[(!(~ pi_reset) && (pi_abort == 1'b1)), (!(~ pi_reset) && !(pi_abort == 1'b1) && (pi_rd_data[hash_idx] == 1'b1 && pi_dest_addr[40] == 1'b1 || pi_multicast == 1'b0))]	
7	`HASH	`MATCH_2	[(!(~ pi_reset) && !(pi_abort == 1'b1) && !(pi_rd_data[hash_idx] == 1'b1 && pi_dest_addr[40] == 1'b1 || pi_multicast == 1'b0))]	
8	`MATCH_2	`IDLE	[(!(~ pi_reset) && (pi_abort == 1'b1)), (!(~ pi_reset) && (po_rd_addr == 4'he) && !(pi_rd_data[47 : 32] == pi_dest_addr[47 : 32])), (!(~ pi_reset) && (po_rd_addr == 4'hf) && !(pi_rd_data[47 : 32] == pi_dest_addr[31 : 16])), (!(~ pi_reset) && (po_rd_addr == 4'h0) && (pi_rd_data[47 : 32] == pi_dest_addr[15 : 0])), (!(~ pi_reset) && (po_rd_addr == 4'h0) && !(pi_rd_data[47 : 32] == pi_dest_addr[15 : 0]))]	

Instances

ip_emac_top : *ip_emac_top*
↪mac_top : *ip_mac_top_g*
↪mac_rx_top : *ip_mac_rx_top_g*
↪rx_hash : *ip_mac_rx_hash_g*

6.30 Module ip_mac_rx_state_g

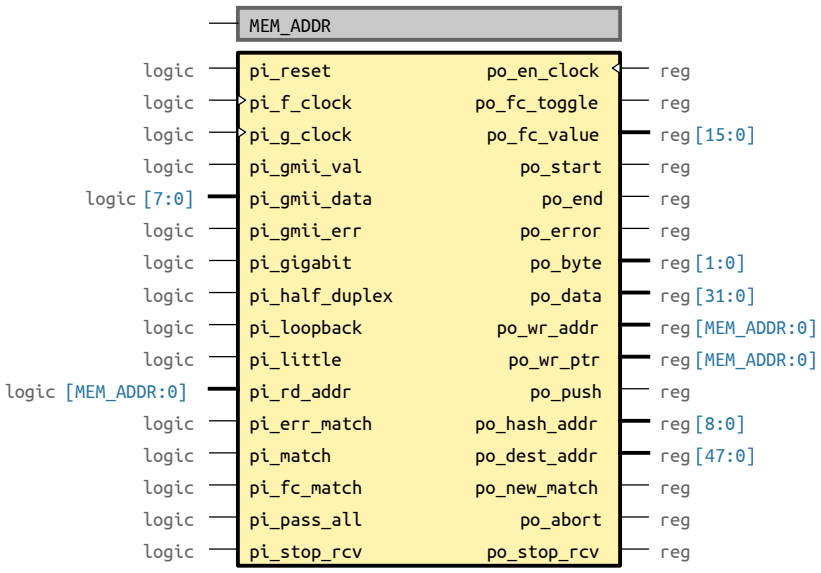

Fig. 30: Block Diagram of ip_mac_rx_state_g

Table 56: Parameters

Name	Default	Description
MEM_ADDR	6	Receive memory address width (9 -> 512 locations, 10->1024)

Table 57: Ports

Name	Type	Direction	Description
pi_reset	wire logic	input	Global Hardware/Software reset (active low)
pi_f_clock	wire logic	input	Free Receive GMII/MII 125/25/2.5 MHz clock (from Clock Manager)
pi_g_clock	wire logic	input	Gated Receive GMII/MII 125/25/2.5 MHz clock (from Clock Manager)
po_en_clock	reg	output	Enable Receive GMII/MII 125/25/2.5 MHz clock (from Clock Manager)
pi_gmii_val	wire logic	input	gmii Data Valid, Data Input Signals and Alignment Error Receive MII/GMII data valid indication (from interface MII block)
pi_gmii_data	wire logic [7 : 0]	input	Receive MII/GMII error indication (from GMII block)

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Table 57 – continued from previous page

Name	Type	Direction	Description
pi_gmii_err	wire logic	input	Receive MII/GMII data (MII data is pi_emac_rx_data[3:0]) (from interface MII block)
pi_gigabit	wire logic	input	Operating 1000 Mbps (Gigabit) mode
pi_half_duplex	wire logic	input	Operating Half Duplex mode
pi_loopback	wire logic	input	Loopback information (frame received in loopback mode)
pi_little	wire logic	input	Little endian data format (used for statistic word translation)
po_fc_toggle	reg	output	Flow control Interface New pause frame received
po_fc_value	reg [15 : 0]	output	Pause time (from FC frame decoding FSM)
po_start	reg	output	Data Path Interface Start of data frame indication
po_end	reg	output	End of data frame indication
po_error	reg	output	Error indication (valid when end of frame or indicate statistic word)
po_byte	reg [1 : 0]	output	Byte enable command, valid only when end of frame
po_data	reg [31 : 0]	output	FIFO Data bus (frame data 32-bit word)
pi_rd_addr	wire logic [*MEM_ADDR* : 0]	input	FIFO Control Interface Used by EMAC Receive State to see the momory state (full/empty/ready)
po_wr_addr	reg [*MEM_ADDR* : 0]	output	Write address (memory write address)
po_wr_ptr	reg [*MEM_ADDR* : 0]	output	Used by RX FIFO to compute the memory state (full/empty/ready)
po_push	reg	output	Write enable command
pi_err_match	wire logic	input	Filterring Interface Address match error
pi_match	wire logic	input	Address match
pi_fc_match	wire logic	input	Address match (control frame address)
pi_pass_all	wire logic	input	Pass all frames (pass bad frames)

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Table 57 – continued from previous page

Name	Type	Direction	Description
po_hash_addr	reg [8 : 0]	output	Hash table index (9-MSB of CRC calculation over 48-bit destination address)
po_dest_addr	reg [47 : 0]	output	Exact match (destination address of the frame)
po_new_match	reg	output	Start a new search (match address, or hash filtering, toggle signal when new match should be prformed)
po_abort	reg	output	Abort search (due to errors)
pi_stop_rcv	wire logic	input	Receive start/stop Receive MAC, receive stopped indication
po_stop_rcv	reg	output	Receive MAC, receive stop command

Always Blocks

`always@(posedge pi_g_clock or negedge pi_reset)`

External Data Memory Addresses

`always@(posedge pi_g_clock or negedge pi_reset)`

FIFO Write State

`always@(posedge pi_g_clock or negedge pi_reset)`

Statistic Word

`always@(posedge pi_g_clock or negedge pi_reset)`

General Counter

`always@(posedge pi_g_clock or negedge pi_reset)`

MAC State Decoder

`always@(posedge pi_f_clock or negedge pi_reset)`

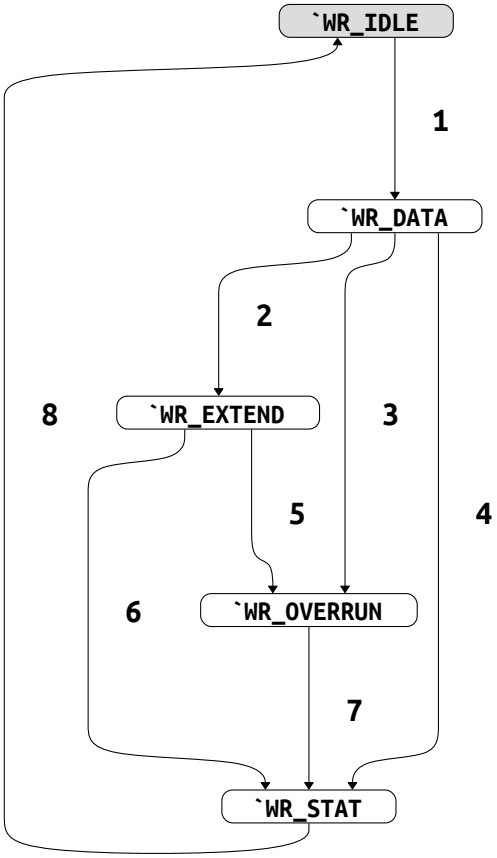

Table 58: FSM Transitions for wr_mac_state

#	Current State	Next State	Condition	Comment
1	`WR_IDLE	`WR_DATA	[(!(~ pi_reset) && (po_stop_rcv == 1'b0 && gmii_valid == 1'b1 && gmii_eop == 1'b0))]	
2	`WR_DATA	`WR_EXTEND	[(!(~ pi_reset) && (gigabit_hd == 1'b1 && extend_ok == 1'b0 && gmii_eop == 1'b1))]	
3	`WR_DATA	`WR_OVERRUN	[(!(~ pi_reset) && !(gigabit_hd == 1'b1 && extend_ok == 1'b0 && gmii_eop == 1'b1) && (gmii_eop == 1'b1) && (full == 1'b1)), (!(~ pi_-reset) && !(gigabit_hd == 1'b1 && extend_ok == 1'b0 && gmii_eop == 1'b1) && !(gmii_eop == 1'b1) && (counter[1 : 0] == 2'b00 && full == 1'b1))]	
4	`WR_DATA	`WR_STAT	[(!(~ pi_reset) && !(gigabit_hd == 1'b1 && extend_ok == 1'b0 && gmii_eop == 1'b1) && (gmii_eop == 1'b1) && !(full == 1'b1))]	

continues on next page

Table 58 – continued from previous page

#	Current State	Next State	Condition	Comment
5	`WR_EXTEND	`WR_OVERRUN	[(!(~ pi_reset) && (extend_ok == 1'b1) && (full == 1'b1)), (!(~ pi_reset) && !(extend_ok == 1'b1) && (gmii_ext == 1'b0) && (full == 1'b1))]	
6	`WR_EXTEND	`WR_STAT	[(!(~ pi_reset) && (extend_ok == 1'b1) && !(full == 1'b1)), (!(~ pi_reset) && !(extend_ok == 1'b1) && (gmii_ext == 1'b0) && !(full == 1'b1))]	
7	`WR_OVERRUN	`WR_STAT	[(!(~ pi_reset) && (full == 1'b0 && gmii_valid == 1'b0 && int_val == 1'b0))]	
8	`WR_STAT	`WR_IDLE	[!(~ pi_reset)]	

Functions

`function logic[31:0] crc32_data8(logic[31:0] crc, logic[7:0] data)`

CRC: 32 DATA: 8, POLY: 104C11DB7 next crc

Parameters

`crc` (*`logic[31:0]`*) -- previous crc

`data` (*`logic[7:0]`*) -- current data

Instances

ip_emac_top : *ip_emac_top*
↪mac_top : *ip_mac_top_g*
↪mac_rx_top : *ip_mac_rx_top_g*
↪rx_state : *ip_mac_rx_state_g* #(.MEM_ADDR(10))

6.31 Module ip_mac_rx_sync_g

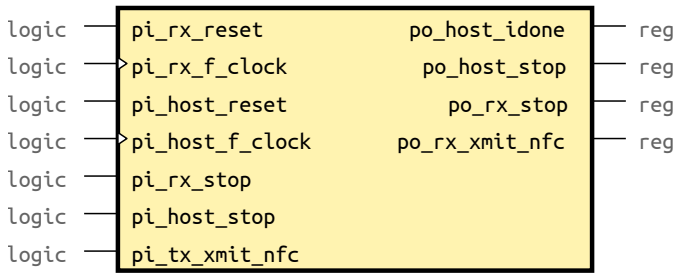

Fig. 31: Block Diagram of ip_mac_rx_sync_g

Table 59: Ports

Name	Type	Direction	Description
pi_rx_reset	wire logic	input	Receive clock and reset Global Hardware/-Software reset (receive clock domain, active low)
pi_rx_f_clock	wire logic	input	Receive GMII/MII 125/25/2.5 MHz clock (from Clock Manager)
po_host_idone	reg	output	Reset done Receive initialisation done (host clock domain)
pi_host_reset	wire logic	input	Host clock and reset Global Hardware/Software reset (host clock domain, active low)
pi_host_f_clock	wire logic	input	Host clock (from Clock Manager)
pi_rx_stop	wire logic	input	Inputs -> Synchronized outputs Receive stop command acknowledge (receive clock domain)
po_host_stop	reg	output	Receive stop command acknowledge (synchronized to host clock domain)
pi_host_stop	wire logic	input	Receive stop command (host clock domain)
po_rx_stop	reg	output	Receive stop command (synchronized to receive clock domain)
pi_tx_xmit_nfc	wire logic	input	Transmit FSM data frame transmit enable (transmit clock domain)
po_rx_xmit_nfc	reg	output	NOTE: This signal is not asserted during flow control frame transmission Transmit FSM data frame transmit enable (synchronized to receive clock domain)

Always Blocks

`always@(posedge pi_rx_f_clock or negedge pi_rx_reset)`

Host to Receive clock domain synchronization

`always@(posedge pi_host_f_clock or negedge pi_host_reset)`

Receive to Host clock domain synchronization

Instances

ip_emac_top : *ip_emac_top*
↪mac_top : *ip_mac_top_g*
↪mac_rx_top : *ip_mac_rx_top_g*
↪rx_sync : *ip_mac_rx_sync_g*

6.32 Module ip_mac_rx_top_g

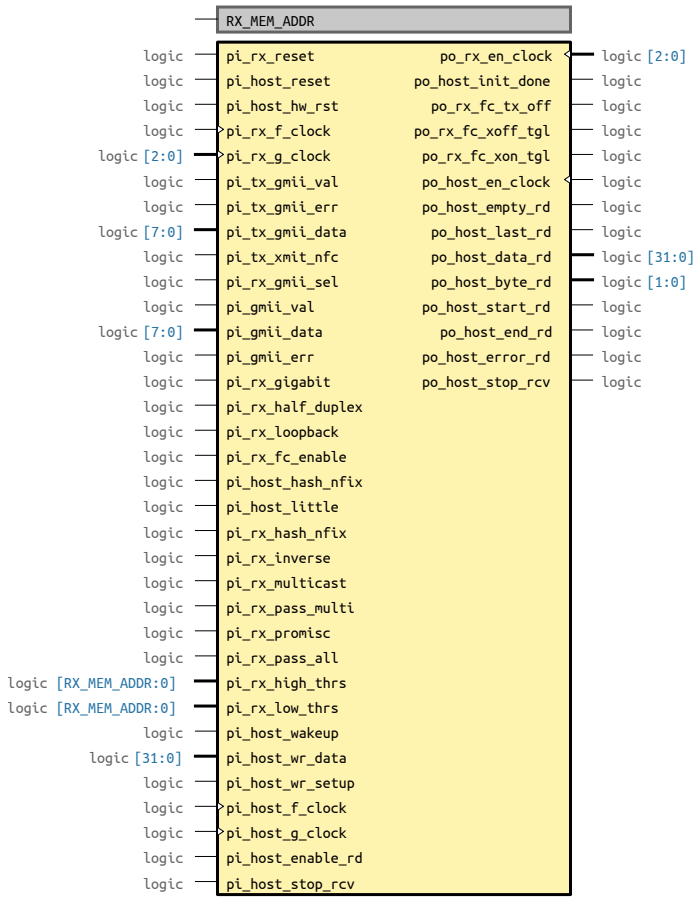

Fig. 32: Block Diagram of ip_mac_rx_top_g

Table 60: Parameters

Name	Default	Description
RX_MEM_ADDR	6	Receive memory address width (9 -> 512 locations, 10->1024)

Table 61: Ports

Name	Type	Direction	Description
pi_rx_reset	wire logic	input	Global Software/Hardware Reset (receive clock domain)
pi_host_reset	wire logic	input	Global Software/Hardware Reset (host clock domain)
pi_host_hw_rst	wire logic	input	Global Hardware Reset (host clock domain)

continues on next page

Table 61 – continued from previous page

Name	Type	Direction	Description
pi_rx_f_clock	wire logic	input	Receive clock Free Receive GMII/MII 125/25/2.5 MHz clock (from Clock Manager)
pi_rx_g_clock	wire logic [2 : 0]	input	Gated Receive GMII/MII 125/25/2.5 MHz clock (from Clock Manager)
po_rx_en_clock	wire logic [2 : 0]	output	Enable Receive GMII/MII 125/25/2.5 MHz clock (from Clock Manager)
po_host_init_done	wire logic	output	Initialisation done Receive initialisation done (host clock domain)
pi_tx_gmii_val	wire logic	input	Loopback GMII/MII Data Valid, Data Input Signals and Alignment Error Loopback MII/GMII data valid indication (from TX)
pi_tx_gmii_err	wire logic	input	Loopback MII/GMII error indication (from TX)
pi_tx_gmii_data	wire logic [7 : 0]	input	Loopback MII/GMII data (MII data is pi_emac_rx_data[3:0]) (from TX)
pi_tx_xmit_nfc	wire logic	input	Transmit full duplex data frame transmit enable pending (non flow control frame is transmitted) Transmit FSM data frame transmit enable (transmit clock domain)
pi_rx_gmii_sel	wire logic	input	NOTE: This signal is not asserted during flow control frame transmission GMII/MII Data Valid, Data Input Signals and Alignment Error Receive GMII data select (demultiplex MII interface indication)
pi_gmii_val	wire logic	input	Note: po_rx_gmii_sel is balanced with the internal receive clock Receive MII/GMII data valid indication (from PHY)
pi_gmii_data	wire logic [7 : 0]	input	Receive MII/GMII error indication (from PHY)
pi_gmii_err	wire logic	input	Receive MII/GMII data (MII data is pi_emac_rx_data[3:0]) (from PHY)
pi_rx_gigabit	wire logic	input	Operating 1000 Mbps (Gigabit) mode
pi_rx_half_duplex	wire logic	input	Operating Half Duplex mode
pi_rx_loopback	wire logic	input	Loopback mode select
pi_rx_fc_enable	wire logic	input	Receive flow control enable (flow control decoding enable)

continues on next page

Table 61 – continued from previous page

Name	Type	Direction	Description
po_rx_fc_tx_off	wire logic	output	Received FC packet (Transmit stop command)
po_rx_fc_xoff_tgl	wire logic	output	(to TX EMAC) insert XOFF flow control information
po_rx_fc_xon_tgl	wire logic	output	(to TX EMAC) insert XON flow control information
pi_host_hash_nfix	wire logic	input	Hash filtering + 1 Address match / 16 Address match
pi_host_little	wire logic	input	Little endian (data path organisation)
pi_rx_hash_nfix	wire logic	input	Configuration Filtering Hash/Exact Hash filtering + 1 Address match / 16 Address match
pi_rx_inverse	wire logic	input	Inverse match filtering mode
pi_rx_multicast	wire logic	input	When asserted the imperfect filtering refers only for multicast addressees
pi_rx_pass_multi	wire logic	input	Pass all multicast addresses
pi_rx_promisc	wire logic	input	Promiscuos Mode (no DA filter)
pi_rx_pass_all	wire logic	input	pass all bad frames (including FC frames)
pi_rx_high_thrs	wire logic [*RX_MEM_ADDR* : 0]	input	from configuration FC high threshold
pi_rx_low_thrs	wire logic [*RX_MEM_ADDR* : 0]	input	from configuration FC low threshold
pi_host_wakeup	wire logic	input	From/To Receive DMA (setup frame) Wake-up internal clock used by the Setup Frame FSM,
pi_host_wr_data	wire logic [31 : 0]	input	should be asserted at least 2 clock cycles (HOST clock) before asserting the pi_host_wr_setup (write enable) and can be deasserted 2 clock cycles after Setup Frame completition Setup Frame data (HOST clock synchronous)
pi_host_wr_setup	wire logic	input	Setup Frame write enable (HOST clock synchronous)
pi_host_f_clock	wire logic	input	Receive data path HOST interface Free HOST interface clock signal
pi_host_g_clock	wire logic	input	Gated Free HOST interface clock signal

continues on next page

Table 61 – continued from previous page

Name	Type	Direction	Description
po_host_en_clock	wire logic	output	Enable Free HOST interface clock signal
pi_host_enable_rd	wire logic	input	Receive MAC data path, HOST enable command
po_host_empty_rd	wire logic	output	Receive MAC data path, HOST FIFO empty indication
po_host_last_rd	wire logic	output	Receive MAC data path, HOST FIFO last location indication
po_host_data_rd	wire logic [31 : 0]	output	Receive MAC data path, HOST data (transmit data)
po_host_byte_rd	wire logic [1 : 0]	output	Receive MAC data path, HOST byte enable (transmit data byte enable)
po_host_start_rd	wire logic	output	Receive MAC data path, HOST start of frame indication
po_host_end_rd	wire logic	output	Receive MAC data path, HOST start of frame indication
po_host_error_rd	wire logic	output	Receive MAC data path, HOST frame error indication (asserted when
pi_host_stop_rcv	wire logic	input	frame is bigger than 64 bytes and receive MAC cannot drop the frame or pass bad frames mode is selected by asserting pi_emac_pass_all) Receive Start/Stop Receive MAC, receive stopped indication (HOST clock synchronous)
po_host_stop_rcv	wire logic	output	Receive MAC, receive stop command (HOST clock synchronous)

Instances

ip_emac_top : *ip_emac_top*
↪mac_top : *ip_mac_top_g*
↪mac_rx_top : *ip_mac_rx_top_g* #(.RX_MEM_ADDR(10))

Submodules

ip_mac_rx_top_g #(.RX_MEM_ADDR(10))
↪cfg_hash : *ip_mac_cfg_hash_g*
↪fc_dec : *ip_mac_fc_dec_g*
↪rx_async : *ip_async_fifo_g* #(.MEM_WIDTH(37))
↪rx_data_dram : *ip_mac_dram_002* #(.MEM_ADDR(10), .MEM_WIDTH(37))
↪rx_dram_hash_0 : *ip_mac_dram_004* #(.MEM_ADDR(4), .MEM_WIDTH(32))
↪rx_dram_hash_1 : *ip_mac_dram_003* #(.MEM_ADDR(4), .MEM_WIDTH(16))
↪rx_endian : *ip_mac_big_endian*
↪rx_fifo : *ip_mac_rx_fifo_g* #(.MEM_ADDR(10))
↪rx_gmii : *ip_mac_rx_gmii_g*
↪rx_hash : *ip_mac_rx_hash_g*

↪rx_state : *ip_mac_rx_state_g* #(.MEM_ADDR(10))
↪rx_sync : *ip_mac_rx_sync_g*

6.33 Module ip_mac_top_g

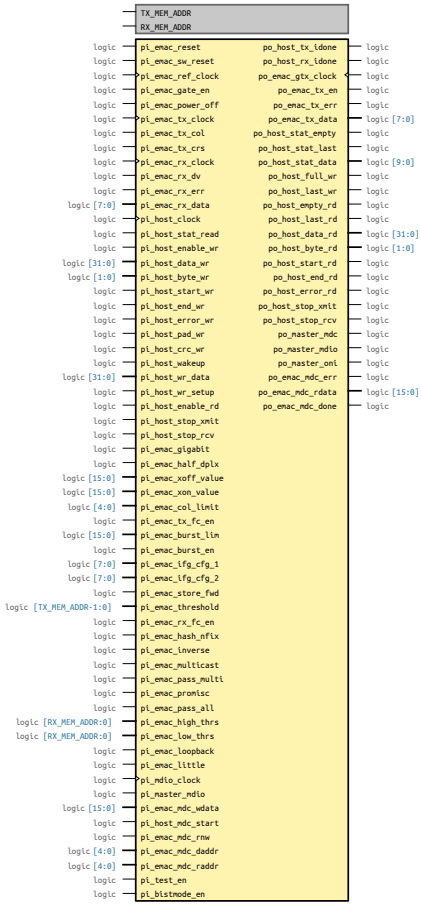

Fig. 33: Block Diagram of ip_mac_top_g

Table 62: Parameters

Name	Default	Description
TX_MEM_ADDR	9	Transmit memory address width (9 -> 512 locations, 10->1024)
RX_MEM_ADDR	6	Receive memory address width (9 -> 512 locations, 10->1024)

Table 63: Ports

Name	Type	Direction	Description
pi_emac_reset	wire logic	input	Global Hardware reset (active low)
pi_emac_sw_reset	wire logic	input	Global Software reset (active high) (should be applied whenever
pi_emac_ref_clock	wire logic	input	GMII 125 MHz reference clock

continues on next page

Table 63 – continued from previous page

Name	Type	Direction	Description
pi_emac_gate_en	wire logic	input	Auto Gating Clock Enable (power saving)
pi_emac_power_off	wire logic	input	Power off (all internal clocks are disabled, except for the HOST clock)
po_host_tx_idone	wire logic	output	Transmit/Receive reset (initialization) done Transmit initialization done (host clock domain)
po_host_rx_idone	wire logic	output	Receive initialization done (host clock domain)
pi_emac_tx_clock	wire logic	input	Transmit GMII/MII interface Transmit MII 25/2.5 MHz clock (from PHY)
po_emac_gtx_clock	wire logic	output	Transmit GMII 125 MHz clock (to PHY)
po_emac_tx_en	wire logic	output	Transmit MII/GMII enable indication (to PHY)
po_emac_tx_err	wire logic	output	Transmit MII/GMII error indication (to PHY)
po_emac_tx_data	wire logic [7 : 0]	output	Transmit MII/GMII data (MII data is po_emac_tx_data[3:0]) (to PHY)
pi_emac_tx_col	wire logic	input	Collision indication (from PHY)
pi_emac_tx_crs	wire logic	input	Carrier Sense indication (from PHY)
pi_emac_rx_clock	wire logic	input	Receive GMII/MII interface Receive GMII/MII 125/25/2.5 MHz clock (from PHY)
pi_emac_rx_dv	wire logic	input	Receive MII/GMII data valid indication (from PHY)
pi_emac_rx_err	wire logic	input	Receive MII/GMII error indication (from PHY)
pi_emac_rx_data	wire logic [7 : 0]	input	Receive MII/GMII data (MII data is pi_emac_rx_data[3:0]) (from PHY)
pi_host_clock	wire logic	input	HOST interface (common) HOST interface clock signal
pi_host_stat_read	wire logic	input	Transmit statistic HOST interface Statistic TDES0 word [8] = jabber,[7] = late collision, [6] = excess collision,[5:2] = collision counter [1] = underrun,[0] = deferred Read statistic word command
po_host_stat_empty	wire logic	output	Statistic FIFO not empty

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Table 63 – continued from previous page

Name	Type	Direction	Description
po_host_stat_last	wire logic	output	Last statistic word indication
po_host_stat_data	wire logic [9 : 0]	output	Statistic TDES0 word data
pi_host_enable_wr	wire logic	input	Tramsmit data path HOST interface Transmit MAC data path, HOST enable command
po_host_full_wr	wire logic	output	Transmit MAC data path, HOST FIFO full indication
po_host_last_wr	wire logic	output	Transmit MAC data path, HOST FIFO last location indication
pi_host_data_wr	wire logic [31 : 0]	input	Transmit MAC data path, HOST data (transmit data)
pi_host_byte_wr	wire logic [1 : 0]	input	Transmit MAC data path, HOST byte enable (transmit data byte enable)
pi_host_start_wr	wire logic	input	Transmit MAC data path, HOST start of frame indication
pi_host_end_wr	wire logic	input	Transmit MAC data path, HOST start of frame indication
pi_host_error_wr	wire logic	input	Unused please check if useful (if not remove)
pi_host_pad_wr	wire logic	input	Transmit MAC data path, HOST padding enable (valid only when pi_host_end_wr)
pi_host_crc_wr	wire logic	input	Transmit MAC data path, HOST crc enable (valid only when pi_host_end_wr)
pi_host_wakeup	wire logic	input	Receive setup frame interface (not affected by software reset, setup frame is written during software reset) Wake-up internal clock used by the Setup Frame FSM,
pi_host_wr_data	wire logic [31 : 0]	input	should be asserted at least 2 clock cycles (HOST clock) before asserting the pi_-host_wr_setup (write enable) and can be deasserted 2 clock cycles after Setup Frame completition Setup Frame data (HOST clock synchronous)
pi_host_wr_setup	wire logic	input	Setup Frame write enable (HOST clock synchronous)
pi_host_enable_rd	wire logic	input	Receive data path HOST interface Receive MAC data path, HOST enable command

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Table 63 – continued from previous page

Name	Type	Direction	Description
po_host_empty_rd	wire logic	output	Receive MAC data path, HOST FIFO empty indication
po_host_last_rd	wire logic	output	Receive MAC data path, HOST FIFO last location indication
po_host_data_rd	wire logic [31 : 0]	output	Receive MAC data path, HOST data (transmit data)
po_host_byte_rd	wire logic [1 : 0]	output	Receive MAC data path, HOST byte enable (transmit data byte enable)
po_host_start_rd	wire logic	output	Receive MAC data path, HOST start of frame indication
po_host_end_rd	wire logic	output	Receive MAC data path, HOST start of frame indication
po_host_error_rd	wire logic	output	Receive MAC data path, HOST frame error indication (asserted when
po_host_stop_xmit	wire logic	output	frame is bigger than 64 bytes and receive MAC cannot drop the frame or pass bad frames mode is selected by asserting pi_emac_pass_all) Start/Stop transmit and receive process Transmit MAC, transmit stopped indication (HOST clock synchronous)
pi_host_stop_xmit	wire logic	input	Transmit MAC, transmit stop command (HOST clock synchronous)
po_host_stop_rcv	wire logic	output	Receive MAC, receive stopped indication (HOST clock synchronous)
pi_host_stop_rcv	wire logic	input	Receive MAC, receive stop command (HOST clock synchronous)
pi_emac_gigabit	wire logic	input	Operating 1000 Mbps (Gigabit) mode
pi_emac_half_dplx	wire logic	input	Operating Half Duplex mode
pi_emac_xoff_value	wire logic [15 : 0]	input	Transmit configuration inputs (require software reset to be active during change) XOFF flow control pause value
pi_emac_xon_value	wire logic [15 : 0]	input	XON flow control pause value
pi_emac_col_limit	wire logic [4 : 0]	input	Half Duplex back pressure collision limit
pi_emac_tx_fc_en	wire logic	input	(maximum collision number during back pressure algorithm) Transmit flow control enable

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Table 63 – continued from previous page

Name	Type	Direction	Description
pi_emac_burst_lim	wire logic [15 : 0]	input	Burst limit (valid only when operating mode is 1000 Mbps)
pi_emac_burst_en	wire logic	input	Burst enable (valid only when operating mode is 1000 Mbps)
pi_emac_ifg_cfg_1	wire logic [7 : 0]	input	Interframe gap part 1 (usually 2/3 from IFG)
pi_emac_ifg_cfg_2	wire logic [7 : 0]	input	Interframe gap part 2 (usually 1/3 from IFG)
pi_emac_store_fwd	wire logic	input	Store and Forward transmit FIFO operating mode
pi_emac_threshold	wire logic [*TX_MEM_ADDR* - 1 : 0]	input	Cut Trough (pi_emac_store_fwd not asserted) FIFO threshold
pi_emac_rx_fc_en	wire logic	input	Receive configuration inputs (require software reset to be active during change) Receive flow control enable (flow control decoding enable)
pi_emac_hash_nfix	wire logic	input	Hash filtering + 1 Address match / 16 Address match
pi_emac_inverse	wire logic	input	Inverse match filtering mode
pi_emac_multicast	wire logic	input	When asserted the imperfect filtering refers only for multicast addressees
pi_emac_pass_multi	wire logic	input	Pass all multicast addresses
pi_emac_promisc	wire logic	input	Promiscuous Mode (no DA filter)
pi_emac_pass_all	wire logic	input	pass all bad frames (including FC frames)
pi_emac_high_thrs	wire logic [*RX_MEM_ADDR* : 0]	input	from configuration FC high threshold
pi_emac_low_thrs	wire logic [*RX_MEM_ADDR* : 0]	input	from configuration FC low threshold
pi_emac_loopback	wire logic	input	Miscelanous configuration inputs (require software reset to be active during change) Loopback mode select
pi_emac_little	wire logic	input	Little endian (data path organization)
pi_mdio_clock	wire logic	input	Management Data Input/Output interface (MDIO) Master MDIO reference clock
po_master_mdc	wire logic	output	Master MDIO output 2.5 MHz clock

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Table 63 – continued from previous page

Name	Type	Direction	Description
pi_master_mdio	wire logic	input	Master MDIO data input line (tri-state buffer outside of the module)
po_master_mdio	wire logic	output	Master MDIO data output line (tri-state buffer outside of the module)
po_master_oni	wire logic	output	Master MDIO direction tri-state buffer control (1 - Output, 0 - Input)
po_emac_mdc_err	wire logic	output	Indicates that a read from MDIO interface is invalid and the
pi_emac_mdc_wdata	wire logic [15 : 0]	input	operation should be retried. This is indicated during a read turn-around cycle when the MDIO slave does not drive the MDIO signal to the low state. MDIO transaction complete. (MDIO clock domain, remain asserted till pi_host_mdc_start is deasserted) MDIO write data (not synchronized, false path, needs to be stable durring pi_host_mdc_start)
po_emac_mdc_rdata	wire logic [15 : 0]	output	MDIO read data (not synchronized, false path, needs to be stable durring pi_host_-mdc_start)
pi_host_mdc_start	wire logic	input	(MDIO clock domain, remain stable till pi_host_mdc_start is deasserted) Setting this bit initiates an MDIO read/write operation (asynchronous,
po_emac_mdc_done	wire logic	output	internally synchronized to MDC clock). Remain asserted till the transaction complete. MDIO transaction complete.
pi_emac_mdc_rnw	wire logic	input	(MDIO clock domain, remain asserted till pi_host_mdc_start is deasserted) This bit indicates the direction of the MDIO operation type:
pi_emac_mdc_daddr	wire logic [4 : 0]	input	0 - MDIO Write operation, 1 - MDIO read operation (not synchronized, false path, needs to be stable during pi_host_mdc_-start) This field is used to specify the device address to be accessed.
pi_emac_mdc_raddr	wire logic [4 : 0]	input	(not synchronized, false path, needs to be stable during pi_host_mdc_start) This field is used to specify the register address to be accessed.

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Table 63 – continued from previous page

Name	Type	Direction	Description
pi_test_en	wire logic	input	(not synchronized, false path, needs to be stable during pi_host_mdc_start) Test and Scan interface signals Test mode enable
pi_bistmode_en	wire logic	input	

Instances

ip_emac_top : *ip_emac_top*
↪mac_top : *ip_mac_top_g* #(.TX_MEM_ADDR(10), .RX_MEM_ADDR(10))

Submodules

ip_mac_top_g #(.TX_MEM_ADDR(10), .RX_MEM_ADDR(10))
↪mac_clk_mng : *ip_mac_clk_mng_g*
↪mac_mdio : *ip_mac_mdio_g*
↪mac_rx_top : *ip_mac_rx_top_g* #(.RX_MEM_ADDR(10))
↪mac_tx_top : *ip_mac_tx_top_g* #(.TX_MEM_ADDR(10))

6.34 Module ip_mac_tx_bkoff_g

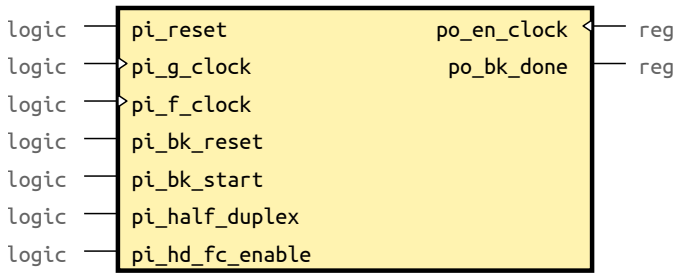

Fig. 34: Block Diagram of ip_mac_tx_bkoff_g

Overview

When a transmission attempt has terminated due to a collision, it is retried by the transmitting CSMA/CD sublayer until either it is successful or a maximum number of attempts have been made and all have terminated due to collisions. Note that all attempts to transmit a given frame are completed before any subsequent outgoing frames are transmitted. The scheduling of the retransmissions is determined by a controlled randomization process called truncated binary exponential backoff.

At the end of enforcing

a collision (jamming), the CSMA/CD sublayer delays before attempting to retransmit the frame. The delay is an integer multiple of 512 bit time slot. The number of slot times to delay before the nth retransmission attempt is chosen as a uniformly distributed random integer r in the range:

-1 < r < 2 power k, where k = min (n, 10)

If all n attempts limit fails, this event is reported as an error. Algorithms used to generate the integer r should be designed to minimize the correlation between the numbers generated by any two stations at any given time.

Note: The values given above define the most aggressive behavior that a station may exhibit in attempting to retransmit after a collision. In the course of implementing the retransmission scheduling procedure, a station may introduce extra delays that will degrade its own throughput, but in no case may a station retransmission scheduling result in a lower average delay between retransmission attempts than the procedure defined above.

Table 64: Ports

Name	Type	Direction	Description
pi_reset	wire logic	input	Global Hardware/Software reset (active low)
pi_g_clock	wire logic	input	Transmit GMII/MII 125/25/2.5 MHz clock (from Clock Manager, gated clock)
pi_f_clock	wire logic	input	Transmit GMII/MII 125/25/2.5 MHz clock (from Clock Manager, free clock)
po_en_clock	reg	output	Transmit GMII/MII 125/25/2.5 MHz clock gated clock enable
pi_bk_reset	wire logic	input	Backoff interface Backoff counter reset command

continues on next page

Table 64 – continued from previous page

Name	Type	Direction	Description
pi_bk_start	wire logic	input	Backoff algorithm start command
pi_half_duplex	wire logic	input	Operating Half Duplex mode
pi_hd_fc_enable	wire logic	input	Half-Duplex Flow Control enable
po_bk_done	reg	output	Backoff done indication

Always Blocks

`always@(posedge pi_g_clock or negedge pi_reset)`

Generate Backoff Done

`always@(posedge pi_f_clock or negedge pi_reset)`

Clock Gating Module

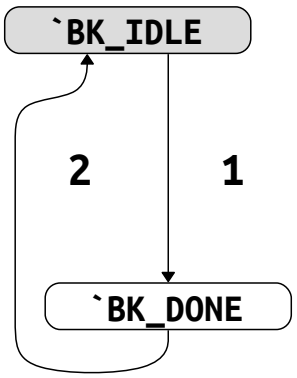

Table 65: FSM Transitions for bk_state

#	Current State	Next State	Condition	Comment
1	`BK_IDLE	`BK_DONE	[(!(~ pi_reset) && (pi_bk_start == 1'b1))]	
2	`BK_DONE	`BK_IDLE	[(!(~ pi_reset) && (bk_ended == slot_cnt && pi_hd_fc_enable == 1'b0)), (!(~ pi_reset) && !(bk_ended == slot_cnt && pi_hd_fc_enable == 1'b0) && (pi_hd_fc_enable == 1'b1))]	

Instances

ip_emac_top : *ip_emac_top*
↪mac_top : *ip_mac_top_g*
↪mac_tx_top : *ip_mac_tx_top_g*
↪tx_bkoff : *ip_mac_tx_bkoff_g*

6.35 Module ip_mac_tx_dpath_g

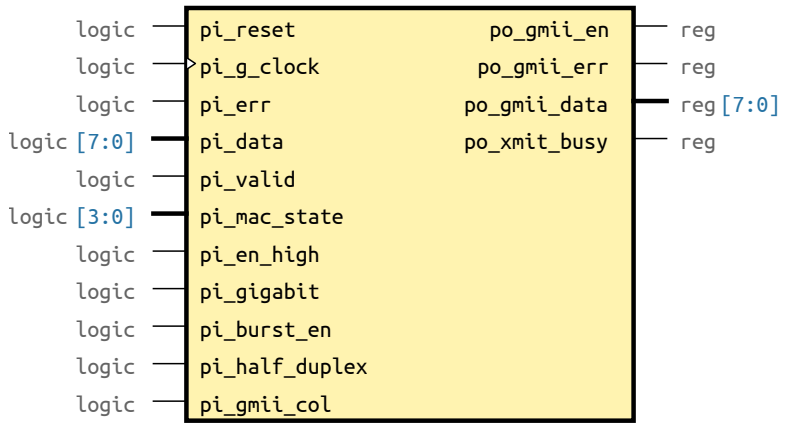

Fig. 35: Block Diagram of ip_mac_tx_dpath_g

Table 66: Ports

Name	Type	Direction	Description
pi_reset	wire logic	input	Global Software/Hardware Reset (transmit clock domain)
pi_g_clock	wire logic	input	Transmit GMII/MII 125/25/2.5 MHz clock (from Clock Manager)
pi_err	wire logic	input	Signals comming in from the data FIFO related to data transfer Error indication
pi_data	wire logic [7 : 0]	input	Data bus (frame data 8-bit word)
pi_valid	wire logic	input	Valid data
pi_mac_state	wire logic [3 : 0]	input	MAC state
pi_en_high	wire logic	input	Enable High (MSB)
pi_gigabit	wire logic	input	Operating 1000 Mbps (Gigabit) mode
pi_burst_en	wire logic	input	Burst enable (valid only when operating mode is 1000 Mbps)
pi_half_duplex	wire logic	input	GMII Interface Half duplex operating mode
pi_gmii_col	wire logic	input	Collision indication (from PHY)
po_gmii_en	reg	output	Transmit MII/GMII enable indication (to PHY)
po_gmii_err	reg	output	Transmit MII/GMII error indication (to PHY)

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Table 66 – continued from previous page

Name	Type	Direction	Description
po_gmii_data	reg [7 : 0]	output	Transmit MII/GMII data (MII data is po_emac_tx_data[3:0]) (to PHY)
po_xmit_busy	reg	output	Used by the defering process (transmit enable ored with transmit error)

Always Blocks

always@(posedge pi_g_clock or negedge pi_reset)

GMII Output Signals Process

Functions

function logic[31:0] crc32_data8(logic[31:0] crc, logic[7:0] data)

CRC: 32 DATA: 8, POLY: 104C11DB7 next crc

Parameters

crc (*logic[31:0]*) -- previous crc

data (*logic[7:0]*) -- current data

Instances

ip_emac_top : *ip_emac_top*
↪mac_top : *ip_mac_top_g*
↪mac_tx_top : *ip_mac_tx_top_g*
↪tx_dpath : *ip_mac_tx_dpath_g*

6.36 Module ip_mac_tx_dsplit_g

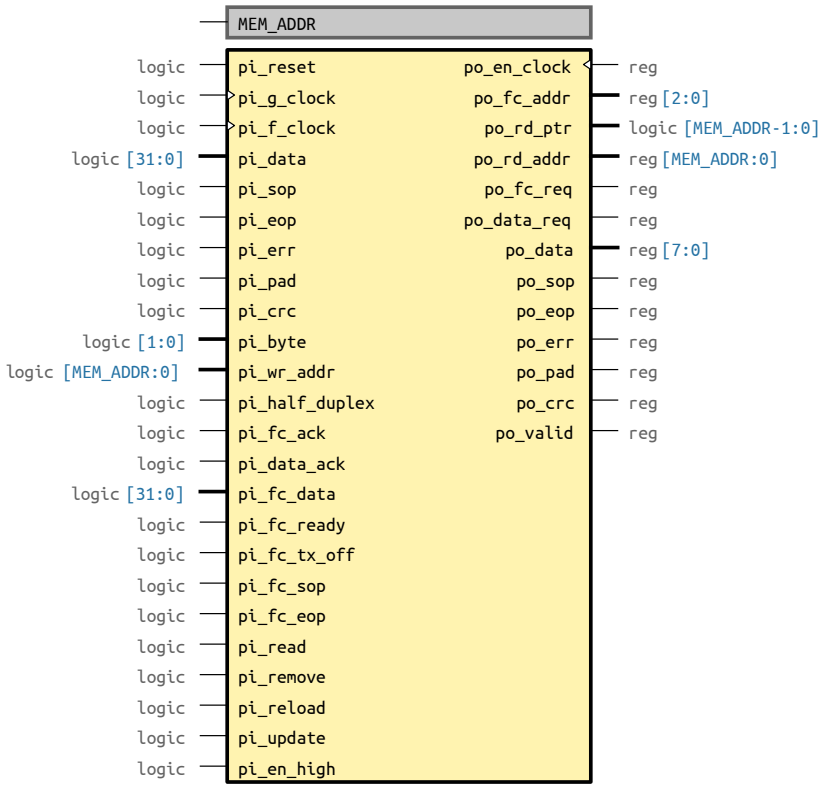

Fig. 36: Block Diagram of ip_mac_tx_dsplit_g

Table 67: Parameters

Name	Default	Description
MEM_ADDR	6	Transmit memory address width (9 -> 512 locations, 10->1024)

Table 68: Ports

Name	Type	Direction	Description
pi_reset	wire logic	input	Global Software/Hardware Reset (transmit clock domain)
pi_g_clock	wire logic	input	Transmit GMII/MII 125/25/2.5 MHz clock (from Clock Manager, gated clock)
pi_f_clock	wire logic	input	Transmit GMII/MII 125/25/2.5 MHz clock (from Clock Manager, free clock)
po_en_clock	reg	output	Transmit GMII/MII 125/25/2.5 MHz clock gated clock enable

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Table 68 – continued from previous page

Name	Type	Direction	Description
pi_data	wire logic [31 : 0]	input	Signals comming in from the data FIFO related to data transfer FIFO Data bus (frame data 32-bit word)
pi_sop	wire logic	input	Start of data frame indication
pi_eop	wire logic	input	End of data frame indication
pi_err	wire logic	input	Error frame indication
pi_pad	wire logic	input	Pad append command, valid only when end of frame (When padding enable
pi_crc	wire logic	input	and frame has less than 64 bytes the CRC is appended regardless of the CRC append setting CRC append command, valid only when end of frame
pi_byte	wire logic [1 : 0]	input	Byte enable information
pi_wr_addr	wire logic [*MEM_ADDR* : 0]	input	Read & Write pointers TX FIFO write address information (used by tx state to determine the
po_fc_addr	reg [2 : 0]	output	FIFO condition full/empty/ready) Flow control read address
pi_half_duplex	wire logic	input	Half duplex flow control enable Half duplex operating mode
po_rd_ptr	wire logic [*MEM_ADDR* - 1 : 0]	output	Output Signals to buffer manager related to data transfer Memory read address
po_rd_addr	reg [*MEM_ADDR* : 0]	output	Used by TX FIFO to compute the memory state (full/empty/ready)
po_fc_req	reg	output	Request & Acknowledge Flow control frame transmit request
po_data_req	reg	output	Data frame transmit request
pi_fc_ack	wire logic	input	Flow control frame transmit acknowledge
pi_data_ack	wire logic	input	Data frame transmit acknowledge
pi_fc_data	wire logic [31 : 0]	input	Flow control generator interface Flow control frame data
pi_fc_ready	wire logic	input	New flow control frame ready
pi_fc_tx_off	wire logic	input	Flow control (pause frame was received, stop transmit command)

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Table 68 – continued from previous page

Name	Type	Direction	Description
pi_fc_sop	wire logic	input	Flow control frame end
pi_fc_eop	wire logic	input	Flow control frame start
pi_read	wire logic	input	Read next data
pi_remove	wire logic	input	Remove current frame (drop frame)
pi_reload	wire logic	input	Reload current frame (retransmit)
pi_update	wire logic	input	Update read pointers (collision window out)
pi_en_high	wire logic	input	Enable High (MSB)
po_data	reg [7 : 0]	output	Signals comming in from the data FIFO related to data transfer Output 8-bit data
po_sop	reg	output	Start of data frame indication
po_eop	reg	output	End of data frame indication
po_err	reg	output	Error frame indication
po_pad	reg	output	Pad append command, valid only when end of frame (When padding enable
po_crc	reg	output	and frame has less than 64 bytes the CRC is appended regardless of the CRC append setting CRC append command, valid only when end of frame
po_valid	reg	output	Valid output data

Always Blocks

always@(read_ptr or pi_wr_addr)

Synchronous write, asynchronous read memory (FIFO output available)

always@(posedge pi_g_clock or negedge pi_reset)

Split Data Counter

always@(posedge pi_g_clock or negedge pi_reset)

Data Output Management

always@(pi_fc_tx_off or pi_sop or prev_valid or pi_fc_ready or pi_fc_sop or unlock_sop)

Data or Flow Control Frame Request (Available)

always@(posedge pi_g_clock or negedge pi_reset)

Delay And Unlock Signal Process

always@(posedge pi_g_clock or negedge pi_reset)

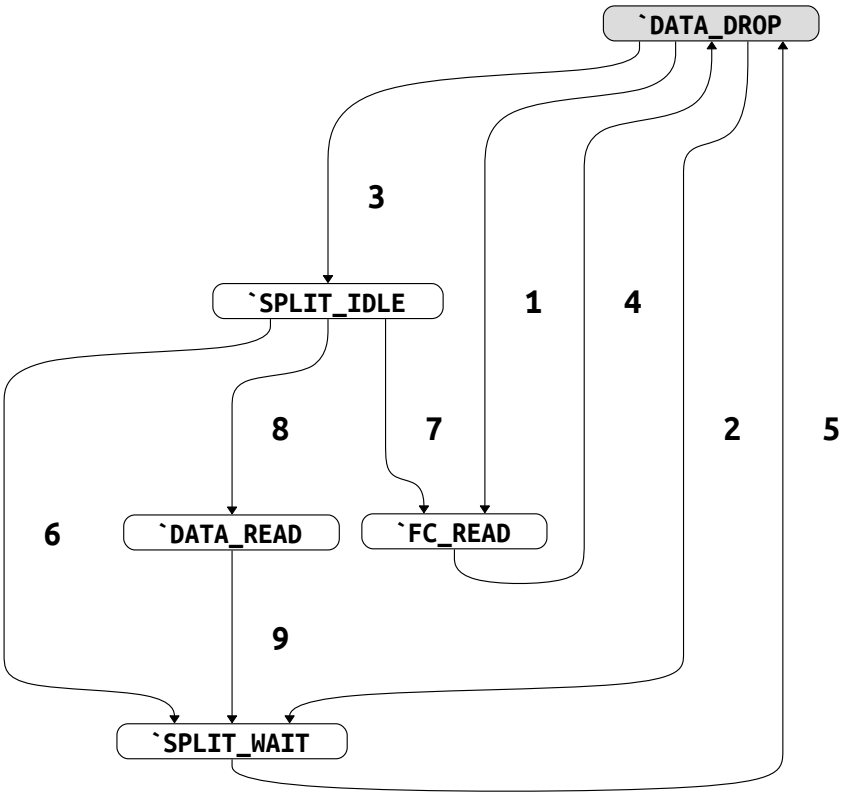

Table 69: FSM Transitions for split_state

#	Current State	Next State	Condition	Comment
1	`DATA_DROP	`FC_READ	[(!(~ pi_reset) && (pi_fc_ack == 1'b1))]	
2	`DATA_DROP	`SPLIT_WAIT	[(!(~ pi_reset) && !(pi_fc_ack == 1'b1) && (reload_frame == 1'b1)), (!(~ pi_reset) && !(pi_fc_ack == 1'b1) && !(reload_frame == 1'b1) && (valid_data == 1'b1 && pi_sop == 1'b0 || unlock_sop == 1'b0))]	
3	`DATA_DROP	`SPLIT_IDLE	[(!(~ pi_reset) && !(pi_fc_ack == 1'b1) && !(reload_frame == 1'b1) && !(valid_data == 1'b1 && pi_sop == 1'b0 || unlock_sop == 1'b0) && (valid_data == 1'b1 && pi_sop == 1'b1 && unlock_sop == 1'b1))]	
4	`FC_READ	`DATA_DROP	[(!(~ pi_reset) && (remove_frame == 1'b1)), (!(~ pi_reset) && !(remove_frame == 1'b1) && (reload_frame == 1'b1)), (!(~ pi_reset) && !(remove_frame == 1'b1) && !(reload_frame == 1'b1) && (po_eop == 1'b1 && pi_read == 1'b1))]	
5	`SPLIT_WAIT	`DATA_DROP	[(!(~ pi_reset) && !(reload_frame == 1'b1))]	

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Table 69 – continued from previous page

#	Current State	Next State	Condition	Comment
6	`SPLIT_IDLE	`SPLIT_WAIT	[(!(~ pi_reset) && (reload_frame == 1'b1))]	
7	`SPLIT_IDLE	`FC_READ	[(!(~ pi_reset) && !(reload_frame == 1'b1) && (pi_fc_ack == 1'b1))]	
8	`SPLIT_IDLE	`DATA_READ	[(!(~ pi_reset) && !(reload_frame == 1'b1) && !(pi_fc_ack == 1'b1) && (pi_data_ack == 1'b1))]	
9	`DATA_READ	`SPLIT_WAIT	[(!(~ pi_reset) && (remove_frame == 1'b1)), (!(~ pi_reset) && !(remove_frame == 1'b1) && (reload_frame == 1'b1)), (!(~ pi_reset) && !(remove_frame == 1'b1) && !(reload_frame == 1'b1) && (po_eop == 1'b1 && valid_data == 1'b1 && pi_read == 1'b1)), (!(~ pi_reset) && !(remove_frame == 1'b1) && !(reload_frame == 1'b1) && !(po_eop == 1'b1 && valid_data == 1'b1 && pi_read == 1'b1) && !(split_cnt == 2'd0 && valid_data == 1'b1 && pi_read == 1'b1) && (po_eop == 1'b1 && valid_data == 1'b0 && pi_read == 1'b1))]	

`always@(posedge pi_f_clock or negedge pi_reset)`

Data or Flow Control Frame Request (Available)

Instances

ip_emac_top : *ip_emac_top*
↪mac_top : *ip_mac_top_g*
↪mac_tx_top : *ip_mac_tx_top_g*
↪tx_dsplit : *ip_mac_tx_dsplit_g* #(.MEM_ADDR(10))

6.37 Module ip_mac_tx_fifo_g

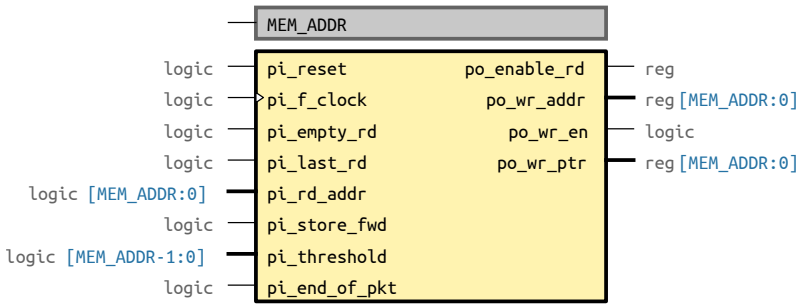

Fig. 37: Block Diagram of ip_mac_tx_fifo_g

Overview

The EMAC Transmit FIFO Control module is responsible to generate all the control signals necessary to transfer the data form the EMAC Asynchronous FIFO module to the EMAC Transmit Memory module. The EMAC Transmit FIFO Control module provides the memory write pointer and the write address, used by the EMAC Transmit module in order to calculate if the memory is ready (actual frame transmission begins after the internal transmit memory had reached either a programmable threshold or after a full frame is contained in the memory). The write address is updated (takes the write pointer value) whenever the memory contains enough data for transmit. The pointer update is made when the number of words of the frame exceeds a programmed threshold value or the entire frame is in the memory.

Table 70: Parameters

Name	Default	Description
MEM_ADDR	6	Transmit memory address width (9 -> 512 locations, 10->1024)

Table 71: Ports

Name	Type	Direction	Description
pi_reset	wire logic	input	Global Hardware/Software reset (active low)
pi_f_clock	wire logic	input	Transmit GMII/MII 125/25/2.5 MHz clock (from Clock Manager, free clock)
pi_empty_rd	wire logic	input	Signals from/to Asynchronous FIFO Asynchronous FIFO empty (no read can be performed)
pi_last_rd	wire logic	input	Asynchronous FIFO last valid location
po_enable_rd	reg	output	Asynchronous FIFO read enable

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Table 71 – continued from previous page

Name	Type	Direction	Description
pi_rd_addr	wire logic [*MEM_ADDR* : 0]	input	Signals from MAC State Machine Used by TX FIFO to compute the memory state (full/empty/ready)
po_wr_addr	reg [*MEM_ADDR* : 0]	output	Used by EMAC Transmit State to compute the memory state (full/empty/ready)
po_wr_en	wire logic	output	Signals to memory (synchronous FIFO block) Write memory enable
po_wr_ptr	reg [*MEM_ADDR* : 0]	output	Write pointer used by the memory to store data
pi_store_fwd	wire logic	input	Configuration Interface Store and forward / Cut trught
pi_threshold	wire logic [*MEM_ADDR* - 1 : 0]	input	Cut trught threshold
pi_end_of_pkt	wire logic	input	The end of packet/frame is stored into memory

Always Blocks

`always@(posedge pi_f_clock or negedge pi_reset)`

Threshold Counter Process

`always@(posedge pi_f_clock or negedge pi_reset)`

Write Address/Pointer Update Process

`always@(posedge pi_f_clock or negedge pi_reset)`

Assign Read async FIFO/Write sync FIFO enable

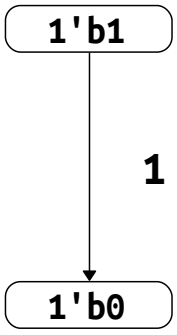

Table 72: FSM Transitions for po_enable_rd

#	Current State	Next State	Condition	Comment
1	1'b1	1'b0	[(!(~ pi_reset) && !(po_wr_ptr[MEM_ADDR] != pi_rd_addr[MEM_ADDR] && po_wr_ptr[MEM_ADDR - 1 : 0] == pi_rd_addr[MEM_ADDR - 1 : 0]) && !(wr_inc[MEM_ADDR] != pi_rd_addr[MEM_ADDR] && wr_inc[MEM_ADDR - 1 : 0] == pi_rd_addr[MEM_ADDR - 1 : 0] && po_wr_en == 1'b1) && !(pi_empty_rd == 1'b1))]	

Instances

ip_emac_top : *ip_emac_top*
↪mac_top : *ip_mac_top_g*
↪mac_tx_top : *ip_mac_tx_top_g*
↪tx_fifo : *ip_mac_tx_fifo_g* #(.MEM_ADDR(10))

6.38 Module ip_mac_tx_fsm_g

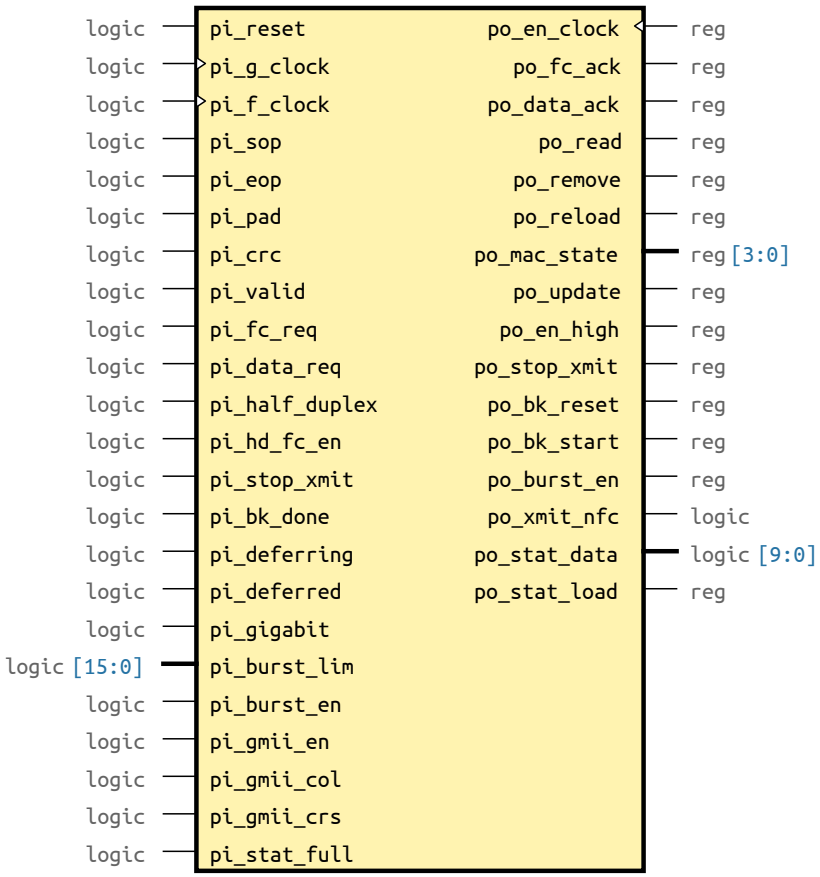

Fig. 38: Block Diagram of ip_mac_tx_fsm_g

Table 73: Ports

Name	Type	Direction	Description
pi_reset	wire logic	input	Global Software/Hardware Reset (transmit clock domain)
pi_g_clock	wire logic	input	Transmit GMII/MII 125/25/2.5 MHz clock (from Clock Manager, gated clock)
pi_f_clock	wire logic	input	Transmit GMII/MII 125/25/2.5 MHz clock (from Clock Manager, free clock)
po_en_clock	reg	output	Transmit GMII/MII 125/25/2.5 MHz clock gated clock enable
pi_sop	wire logic	input	Signals comming in from the data FIFO related to data transfer Start of data frame indication
pi_eop	wire logic	input	End of data frame indication

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Table 73 – continued from previous page

Name	Type	Direction	Description
pi_pad	wire logic	input	Pad append command, valid only when end of frame (When padding enable
pi_crc	wire logic	input	and frame has less than 64 bytes the CRC is appended regardless of the CRC append setting CRC append command, valid only when end of frame
pi_valid	wire logic	input	Valid data
pi_fc_req	wire logic	input	Request & Acknowledge Flow control frame transmit request
pi_data_req	wire logic	input	Data frame transmit request
po_fc_ack	reg	output	Flow control frame transmit acknowledge
po_data_ack	reg	output	Data frame transmit acknowledge
po_read	reg	output	Read & Retransmit & Drop current frame Read next data
po_remove	reg	output	Remove current frame (drop frame)
po_reload	reg	output	Reload current frame (retransmit)
po_mac_state	reg [3 : 0]	output	Transmit FSM state Transmit FSM state current
po_update	reg	output	Collision window Collision window (update read pointer)
po_en_high	reg	output	Enable increment counter
pi_half_duplex	wire logic	input	Half duplex flow control enable Half duplex operating mode
pi_hd_fc_en	wire logic	input	Half-Duplex Flow Control enable
pi_stop_xmit	wire logic	input	Transmit start/stop Transmit EMAC stop command
po_stop_xmit	reg	output	Transmit EMAC stopped
po_bk_reset	reg	output	Control Signals Related to the Backoff Block Backoff counter reset command
po_bk_start	reg	output	Backoff algorithm start command
pi_bk_done	wire logic	input	Backoff done indication

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Table 73 – continued from previous page

Name	Type	Direction	Description
pi_deferring	wire logic	input	Control Signal from the deferral counter Defer current transmition (when asserted high)
pi_deferred	wire logic	input	Deferred frame statistic information (asserted for one cycle)
pi_gigabit	wire logic	input	Operating 1000 Mbps (Gigabit) mode
pi_burst_lim	wire logic [15 : 0]	input	Burst limit (valid only when operating mode is 1000 Mbps)
pi_burst_en	wire logic	input	Burst enable (valid only when operating mode is 1000 Mbps)
po_burst_en	reg	output	Burst enable (valid only when operating mode is 1000 Mbps)
pi_gmii_en	wire logic	input	GMII Interface Transmit MII/GMII enable indication (to PHY)
pi_gmii_col	wire logic	input	Collision indication (from PHY)
pi_gmii_crs	wire logic	input	Carrier Sense indication (from PHY)
po_xmit_nfc	wire logic	output	(compensate the tx_gmii latency, connected to po_gmii_en on MII/GMII module) Transmit full duplex data frame transmit enable pending (non flow control frame is transmitted) Transmit FSM data frame transmit enable
pi_stat_full	wire logic	input	NOTE: This signal is not asserted during flow control frame transmission Statistic related signals Statistic FIFO full
po_stat_data	wire logic [9 : 0]	output	Statistic FIFO data
po_stat_load	reg	output	Statistic FIFO write enable signal

Always Blocks

`always@(posedge pi_g_clock or negedge pi_reset)`

Carrier Sense Delay Process

`always@(posedge pi_g_clock or negedge pi_reset)`

General Counter 64 bytes and 512 bytes Detect

`always@(posedge pi_g_clock or negedge pi_reset)`

FIFO pointers Management

`always@(posedge pi_g_clock or negedge pi_reset)`

Backoff And Statistic Signals Generation

`always@(posedge pi_g_clock or negedge pi_reset)`

Backoff And Statistic Signals Generation

always@(posedge pi_g_clock or negedge pi_reset)

MAC State Decoder

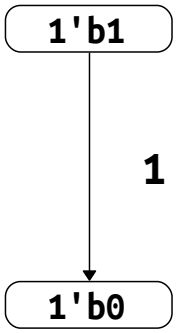

Table 74: FSM Transitions for force_col

#	Current State	Next State	Condition	Comment
1	1'b1	1'b0	[(!(~ pi_reset) && (po_mac_state == 4'h1)), (!(~ pi_reset) && (po_mac_-state == 4'h1))]	

always@(posedge pi_f_clock or negedge pi_reset)

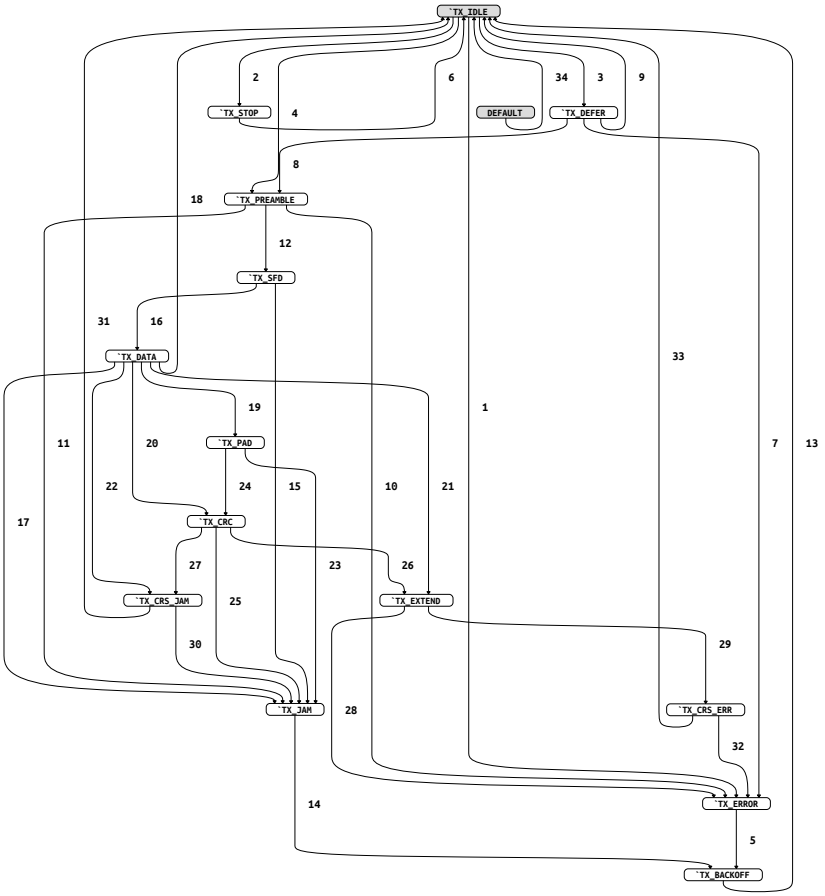

Table 75: FSM Transitions for po_mac_state

#	Current State	Next State	Condition	Comment
1	`TX_IDLE	`TX_ERROR	[(!(~ pi_reset) && (gmii_col == 1'b1 && po_burst_en == 1'b1))]	
2	`TX_IDLE	`TX_STOP	[(!(~ pi_reset) && !(gmii_col == 1'b1 && po_burst_en == 1'b1) && (stop_xmit == 1'b1))]	
3	`TX_IDLE	`TX_DEFER	[(!(~ pi_reset) && !(gmii_col == 1'b1 && po_burst_en == 1'b1) && !(stop_xmit == 1'b1) && (pi_fc_req == 1'b1)), (!(~ pi_reset) && !(gmii_col == 1'b1 && po_burst_en == 1'b1) && !(stop_xmit == 1'b1) && !(pi_fc_req == 1'b1) && (pi_data_req == 1'b1))]	
4	`TX_IDLE	`TX_PREAMBLE	[(!(~ pi_reset) && !(gmii_col == 1'b1 && po_burst_en == 1'b1) && !(stop_xmit == 1'b1) && !(pi_fc_req == 1'b1) && !(pi_data_req == 1'b1) && (gmii_crs == 1'b1 && gmii_crs_del == 1'b0 && pi_hd_fc_en == 1'b1))]	
5	`TX_ERROR	`TX_BACKOFF	[(!(~ pi_reset) && ({counter[1 : 0], po_en_high} == {1'b1, ~ pi_gigabit, pi_gigabit}))]	
6	`TX_STOP	`TX_IDLE	[(!(~ pi_reset) && (stop_xmit == 1'b0))]	
7	`TX_DEFER	`TX_ERROR	[(!(~ pi_reset) && (gmii_col == 1'b1 && po_burst_en == 1'b1))]	
8	`TX_DEFER	`TX_PREAMBLE	[(!(~ pi_reset) && !(gmii_col == 1'b1 && po_burst_en == 1'b1) && (pi_deferring == 1'b0 && pi_sop == 1'b1)), (!(~ pi_reset) && !(gmii_col == 1'b1 && po_burst_en == 1'b1) && !(pi_deferring == 1'b0 && pi_sop == 1'b1) && !(pi_deferring == 1'b0 && force_col == 1'b1) && (pi_deferring == 1'b0))]	
9	`TX_DEFER	`TX_IDLE	[(!(~ pi_reset) && !(gmii_col == 1'b1 && po_burst_en == 1'b1) && !(pi_deferring == 1'b0 && pi_sop == 1'b1) && (pi_deferring == 1'b0 && force_col == 1'b1))]	
10	`TX_PREAMBLE	`TX_ERROR	[(!(~ pi_reset) && (gmii_col == 1'b1 && pi_gmii_en == 1'b0))]	
11	`TX_PREAMBLE	`TX_JAM	[(!(~ pi_reset) && !(gmii_col == 1'b1 && pi_gmii_en == 1'b0) && (gmii_col == 1'b1))]	
12	`TX_PREAMBLE	`TX_SFD	[(!(~ pi_reset) && !(gmii_col == 1'b1 && pi_gmii_en == 1'b0) && !(gmii_col == 1'b1) && ({counter[2 : 1], po_en_high} == {2'd3, 1'b1}))]	

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Table 75 – continued from previous page

#	Current State	Next State	Condition	Comment
13	`TX_BACKOFF	`TX_IDLE	[(!(~ pi_reset) && (col_counter[4] == 1'b1 || window_out == 1'b1)), (!(~ pi_reset) && !(col_counter[4] == 1'b1 || window_out == 1'b1) && (pi_bk_done == 1'b1 && po_bk_-start == 1'b0))]	
14	`TX_JAM	`TX_BACKOFF	[(!(~ pi_reset) && ({counter[1 : 0], po_en_high} == {1'b1, ~ pi_gigabit | force_col, pi_gigabit | force_col}))]	
15	`TX_SFD	`TX_JAM	[(!(~ pi_reset) && (po_en_high == 1'b1 && force_col == 1'b1 || gmii_-col == 1'b1))]	
16	`TX_SFD	`TX_DATA	[(!(~ pi_reset) && !(po_en_high == 1'b1 && force_col == 1'b1 || gmii_-col == 1'b1) && (po_en_high == 1'b1))]	
17	`TX_DATA	`TX_JAM	[(!(~ pi_reset) && (gmii_col == 1'b1))]	
18	`TX_DATA	`TX_IDLE	[(!(~ pi_reset) && !(gmii_col == 1'b1) && (counter[14] == 1'b1 && counter[0] == 1'b1 && po_en_high == 1'b1)), (!(~ pi_reset) && !(gmii_-col == 1'b1) && !(counter[14] == 1'b1 && counter[0] == 1'b1 && po_-en_high == 1'b1) && (pi_valid == 1'b0 && po_en_high == 1'b1))]	
19	`TX_DATA	`TX_PAD	[(!(~ pi_reset) && !(gmii_col == 1'b1) && !(counter[14] == 1'b1 && counter[0] == 1'b1 && po_en_high == 1'b1) && !(pi_valid == 1'b0 && po_en_high == 1'b1) && (int_eop == 1'b1 && count_60 == 1'b0 && pi_pad == 1'b1 && po_en_high == 1'b1))]	
20	`TX_DATA	`TX_CRC	[(!(~ pi_reset) && !(gmii_col == 1'b1) && !(counter[14] == 1'b1 && counter[0] == 1'b1 && po_en_high == 1'b1) && !(pi_valid == 1'b0 && po_en_high == 1'b1) && !(int_-eop == 1'b1 && count_60 == 1'b0 && pi_pad == 1'b1 && po_en_high == 1'b1) && (int_eop == 1'b1 && pi_crc == 1'b1 && po_en_high == 1'b1))]	

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Table 75 – continued from previous page

#	Current State	Next State	Condition	Comment
21	`TX_DATA	`TX_EXTEND	[(!(~ pi_reset) && !(gmii_col == 1'b1) && !(counter[14] == 1'b1 && counter[0] == 1'b1 && po_en_high == 1'b1) && !(pi_valid == 1'b0 && po_en_high == 1'b1) && !(int_eop == 1'b1 && count_60 == 1'b0 && pi_pad == 1'b1 && po_en_high == 1'b1) && !(int_eop == 1'b1 && pi_crc == 1'b1 && po_en_high == 1'b1) && (int_eop == 1'b1 && count_512 == 1'b0 && burst_begin == 1'b1 && pi_half_duplex == 1'b1))]	
22	`TX_DATA	`TX_CRS_JAM	[(!(~ pi_reset) && !(gmii_col == 1'b1) && !(counter[14] == 1'b1 && counter[0] == 1'b1 && po_en_high == 1'b1) && !(pi_valid == 1'b0 && po_en_high == 1'b1) && !(int_eop == 1'b1 && count_60 == 1'b0 && pi_pad == 1'b1 && po_en_high == 1'b1) && !(int_eop == 1'b1 && pi_crc == 1'b1 && po_en_high == 1'b1) && !(int_eop == 1'b1 && count_512 == 1'b0 && burst_begin == 1'b1 && pi_half_duplex == 1'b1) && (int_eop == 1'b1 && po_en_high == 1'b1))]	
23	`TX_PAD	`TX_JAM	[(!(~ pi_reset) && (gmii_col == 1'b1))]	
24	`TX_PAD	`TX_CRC	[(!(~ pi_reset) && !(gmii_col == 1'b1) && (count_60 == 1'b1 && po_en_high == 1'b1))]	
25	`TX_CRC	`TX_JAM	[(!(~ pi_reset) && (gmii_col == 1'b1))]	
26	`TX_CRC	`TX_EXTEND	[(!(~ pi_reset) && !(gmii_col == 1'b1) && (crc_counter == 2'd3 && count_512 == 1'b0 && burst_begin == 1'b1 && pi_half_duplex == 1'b1))]	
27	`TX_CRC	`TX_CRS_JAM	[(!(~ pi_reset) && !(gmii_col == 1'b1) && !(crc_counter == 2'd3 && count_512 == 1'b0 && burst_begin == 1'b1 && pi_half_duplex == 1'b1) && ({crc_counter, po_en_high} == {2'd3, 1'b1}))]	
28	`TX_EXTEND	`TX_ERROR	[(!(~ pi_reset) && (gmii_col == 1'b1))]	
29	`TX_EXTEND	`TX_CRS_ERR	[(!(~ pi_reset) && !(gmii_col == 1'b1) && (count_512 == 1'b1))]	
30	`TX_CRS_JAM	`TX_JAM	[(!(~ pi_reset) && (gmii_col == 1'b1))]	
31	`TX_CRS_JAM	`TX_IDLE	[(!(~ pi_reset) && !(gmii_col == 1'b1) && (gmii_crs == 1'b0 || po_burst_en == 1'b1))]	
32	`TX_CRS_ERR	`TX_ERROR	[(!(~ pi_reset) && (gmii_col == 1'b1))]	

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Table 75 – continued from previous page

#	Current State	Next State	Condition	Comment
33	`TX_CRS_ERR	`TX_IDLE	[(!(~ pi_reset) && !(gmii_col == 1'b1) && (gmii_crs == 1'b0 || po_burst_en == 1'b1))]	
34	default	`TX_IDLE	[!(~ pi_reset)]	

Instances

ip_emac_top : *ip_emac_top*
↪mac_top : *ip_mac_top_g*
↪mac_tx_top : *ip_mac_tx_top_g*
↪tx_fsm : *ip_mac_tx_fsm_g*

6.39 Module ip_mac_tx_gmii_g

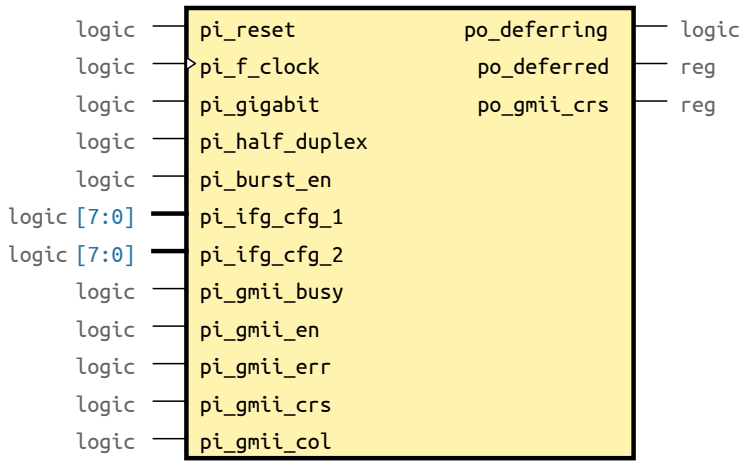

Fig. 39: Block Diagram of ip_mac_tx_gmii_g

Overview

Frames are transmitted over the EMAC MII/GMII interface with an interframe gap which is specified by the IEEE 802.3-2002 standard to be 96 bit times (9.6 us for 10 Mbps, 0.96 us for 100 Mbps, 0.096 us for 1000 Mbps). This is a minimum value and may be increased with a resulting decrease in throughput (results in a less aggressive approach to gain access to a shared Ethernet bus). The process for deferring the transmission is different for half-duplex and full-duplex systems and is as follows:

Half-Duplex Even when it has nothing to transmit, the EMAC monitors the bus for traffic by watching the carrier sense signal from the external PHY. Whenever the bus is busy, the EMAC defers to the passing frame by delaying any pending transmission of its own. After the last bit of the passing frame (when carrier sense signal changes from true to false), the EMAC starts the timing of the interframe gap. The EMAC will reset the interframe gap timer if carrier sense becomes true during the first period defined by the IFG1. The IEEE 802.3-2002 standard states that this should be the first 2/3 of the interframe gap interval (64 bit times) but may be shorter and as small as zero. The EMAC will not reset the interframe gap timer if carrier sense becomes true during the period defined by the second IFG2 field to ensure fair access to the bus. The IEEE 802.3-2002 standard states that this should be the last 1/3 of the interframe gap timing interval (32 bit times) but may be longer and as large as the whole interframe gap time.

Full-Duplex The EMAC does not use the carrier sense signal from the external PHY when in full duplex mode since the bus is not shared and only needs to monitor its own transmissions. After the last bit of an EMAC transmission, the EMAC starts the interframe gap timer and defers transmissions until it has reached the value represented by the combination of the IFG1 and IFG2.

The EMAC Transmit MII/GMII module is responsible also to demultilex the GMII interface signals coming from EMAC Transmit State Machine into MII format (nibble oriented) when 10/100 Mbps operating mode is selected or to pass the GMII signal to the output when 1000 Mbps operating mode. The GMII/MII block is responsible to register the input signals comming from the physical layer, and synchronize the carrier sense indication (two DFF's are required since the carrier sense is an asynchronous input)

Table 76: Ports

Name	Type	Direction	Description
pi_reset	wire logic	input	Global Hardware/Software reset (active low)
pi_f_clock	wire logic	input	Transmit GMII/MII 125/25/2.5 MHz clock (from Clock Manager)
pi_gigabit	wire logic	input	Operating 1000 Mbps (Gigabit) mode
pi_half_duplex	wire logic	input	Defer interface Operating Half Duplex mode
pi_burst_en	wire logic	input	Burst enable (valid only when operating mode is 1000 Mbps)
pi_ifg_cfg_1	wire logic [7 : 0]	input	Interframe gap part 1 (usualy 2/3 from IFG)
pi_ifg_cfg_2	wire logic [7 : 0]	input	Interframe gap part 2 (usualy 1/3 from IFG)
po_deferring	wire logic	output	Defer current transmition (when asserted high)
po_deferred	reg	output	Statistic information (frame was deferred)
pi_gmii_busy	wire logic	input	Tx MAC state interface
pi_gmii_en	wire logic	input	Transmit GMII enable indication
pi_gmii_err	wire logic	input	Transmit GMII error indication
po_gmii_crs	reg	output	Carrier Sense indication
pi_gmii_crs	wire logic	input	MII Transmit Enable and Data Output Signals, Carrier Sense and Colision Indicators Carrier Sense indication Asynchronous input (2 DFF required for synchronization) (from PHY)
pi_gmii_col	wire logic	input	Collision indication (from PHY)

Always Blocks

`always@(posedge pi_f_clock or negedge pi_reset)`

Input MII/GMII Signals Synchronization

`always@(negedge pi_f_clock or negedge pi_reset)`

Falling edge (inverted clock used for first synchronization DFF) always @(posedge pi_i_clock or negedge pi_reset)

`always@(defer_state or pi_gmii_en or gmii_col or pi_half_duplex or gmii_crs or pi_gmii_err or pi_gmii_busy or counter or pi_burst_en or gmii_busy_del)`

Defer MII/GMII FSM

`always@(posedge pi_f_clock or negedge pi_reset)`

Defer Counter

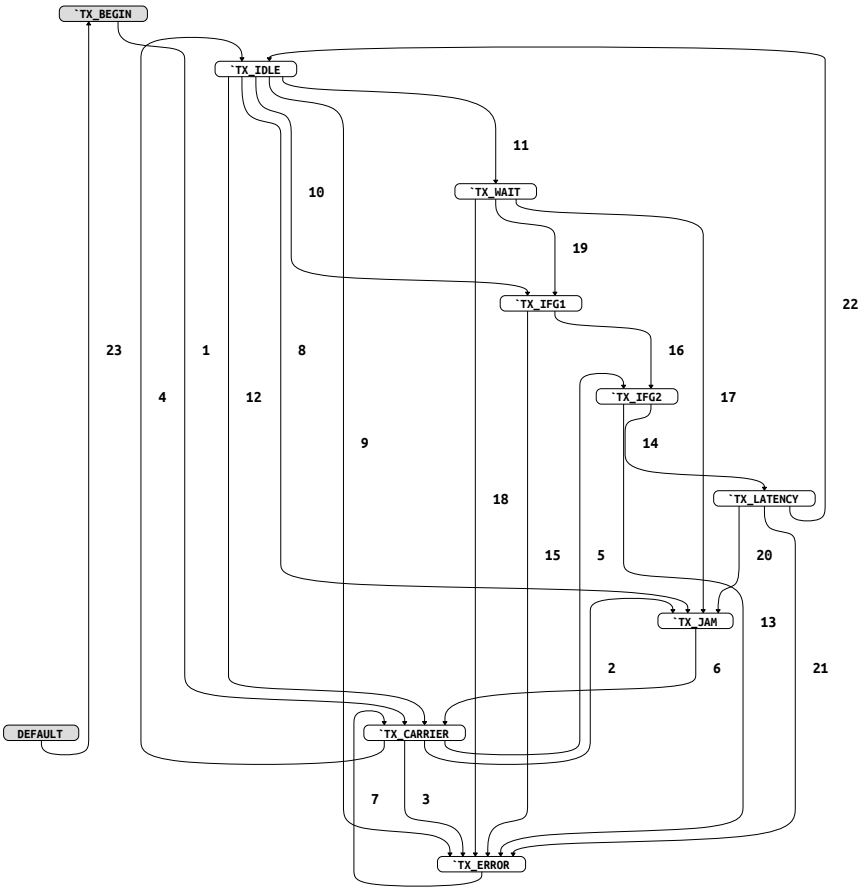

Table 77: FSM Transitions for defer_state

#	Current State	Next State	Condition	Comment
1	`TX_BEGIN	`TX_CARRIER	[EMPTY]	
2	`TX_CARRIER	`TX_JAM	[(pi_gmii_en == 1'b1 && pi_gmii_busy == 1'b1 && gmii_col == 1'b1)]	
3	`TX_CARRIER	`TX_ERROR	[(!(pi_gmii_en == 1'b1 && pi_gmii_busy == 1'b1 && gmii_col == 1'b1) && (pi_gmii_err == 1'b1 && pi_gmii_busy == 1'b1 && gmii_col == 1'b1))]	
4	`TX_CARRIER	`TX_IDLE	[(!(pi_gmii_en == 1'b1 && pi_gmii_busy == 1'b1 && gmii_col == 1'b1) && !(pi_gmii_err == 1'b1 && pi_gmii_busy == 1'b1 && gmii_col == 1'b1) && (pi_gmii_busy == 1'b1))]	
5	`TX_CARRIER	`TX_IFG2	[(!(pi_gmii_en == 1'b1 && pi_gmii_busy == 1'b1 && gmii_col == 1'b1) && !(pi_gmii_err == 1'b1 && pi_gmii_busy == 1'b1 && gmii_col == 1'b1) && !(pi_gmii_busy == 1'b1) && !(gmii_crs == 1'b1) && (counter == 9'd0))]	
6	`TX_JAM	`TX_CARRIER	[(counter == 9'd1)]	
7	`TX_ERROR	`TX_CARRIER	[(counter == 9'd1)]	

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Table 77 – continued from previous page

#	Current State	Next State	Condition	Comment
8	`TX_IDLE	`TX_JAM	[(pi_gmii_en == 1'b1 && gmii_col == 1'b1)]	
9	`TX_IDLE	`TX_ERROR	[(!(pi_gmii_en == 1'b1 && gmii_col == 1'b1) && (pi_gmii_err == 1'b1 && gmii_col == 1'b1))]	
10	`TX_IDLE	`TX_IFG1	[(!(pi_gmii_en == 1'b1 && gmii_col == 1'b1) && !(pi_gmii_err == 1'b1 && gmii_col == 1'b1) && !(pi_-gmii_busy == 1'b1) && (pi_gmii_-busy == 1'b0 && gmii_busy_del == 1'b1 && gmii_crs == 1'b0 || pi_-burst_en == 1'b1))]	
11	`TX_IDLE	`TX_WAIT	[(!(pi_gmii_en == 1'b1 && gmii_col == 1'b1) && !(pi_gmii_err == 1'b1 && gmii_col == 1'b1) && !(pi_-gmii_busy == 1'b1) && !(pi_gmii_-busy == 1'b0 && gmii_busy_del == 1'b1 && gmii_crs == 1'b0 || pi_-burst_en == 1'b1) && (pi_gmii_-busy == 1'b0 && gmii_busy_del == 1'b1))]	
12	`TX_IDLE	`TX_CARRIER	[(!(pi_gmii_en == 1'b1 && gmii_col == 1'b1) && !(pi_gmii_err == 1'b1 && gmii_col == 1'b1) && !(pi_-gmii_busy == 1'b1) && !(pi_gmii_-busy == 1'b0 && gmii_busy_del == 1'b1 && gmii_crs == 1'b0 || pi_-burst_en == 1'b1) && !(pi_gmii_-busy == 1'b0 && gmii_busy_del == 1'b1) && (gmii_crs == 1'b1 && pi_-gmii_en == 1'b0 && pi_gmii_err == 1'b0))]	
13	`TX_IFG2	`TX_ERROR	[(pi_gmii_err == 1'b1 && gmii_col == 1'b1)]	
14	`TX_IFG2	`TX_LATENCY	[(!(pi_gmii_err == 1'b1 && gmii_col == 1'b1) && (counter == 9'd0))]	
15	`TX_IFG1	`TX_ERROR	[(pi_gmii_err == 1'b1 && gmii_col == 1'b1)]	
16	`TX_IFG1	`TX_IFG2	[(!(pi_gmii_err == 1'b1 && gmii_col == 1'b1) && (counter == 9'd0))]	
17	`TX_WAIT	`TX_JAM	[(pi_gmii_en == 1'b1 && gmii_col == 1'b1)]	
18	`TX_WAIT	`TX_ERROR	[(!(pi_gmii_en == 1'b1 && gmii_col == 1'b1) && (pi_gmii_err == 1'b1 && gmii_col == 1'b1))]	
19	`TX_WAIT	`TX_IFG1	[(!(pi_gmii_en == 1'b1 && gmii_col == 1'b1) && !(pi_gmii_err == 1'b1 && gmii_col == 1'b1) && (gmii_crs == 1'b0))]	
20	`TX_LATENCY	`TX_JAM	[(pi_gmii_en == 1'b1 && gmii_col == 1'b1)]	
21	`TX_LATENCY	`TX_ERROR	[(!(pi_gmii_en == 1'b1 && gmii_col == 1'b1) && (pi_gmii_err == 1'b1 && gmii_col == 1'b1))]	

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Table 77 – continued from previous page

#	Current State	Next State	Condition	Comment
22	`TX_LATENCY	`TX_IDLE	[(!(pi_gmii_en == 1'b1 && gmii_col == 1'b1) && !(pi_gmii_err == 1'b1 && gmii_col == 1'b1) && (counter == 9'd0))]	
23	default	`TX_BEGIN	[EMPTY]	

Instances

ip_emac_top : *ip_emac_top*
↪mac_top : *ip_mac_top_g*
↪mac_tx_top : *ip_mac_tx_top_g*
↪tx_gmii : *ip_mac_tx_gmii_g*

6.40 Module ip_mac_tx_sync_g

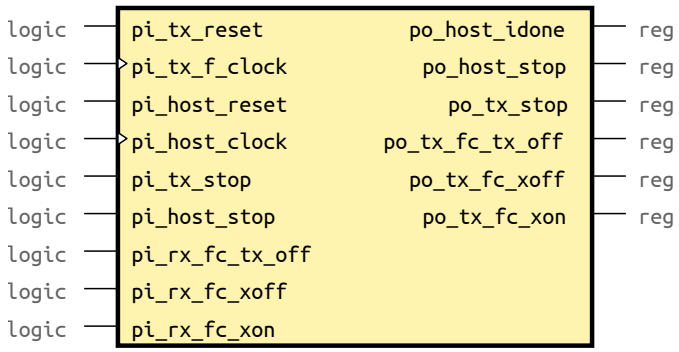

Fig. 40: Block Diagram of ip_mac_tx_sync_g

Overview

The EMAC Transmit Synchronization module is responsible to synchronize all the control signals necessary to control the functionality of the transmit clock domain modules. Also the signals generated by the transmit modules and needed by the host clock domain modules are synchronized by the EMAC Transmit Synchronization module to host clock domain. In order to avoid the metastability of the output signal the synchronization from one clock domain to another will require two DFF's. The host and transmit clocks used by the synchronization module are free running clocks, since there is no possibility to generate synchronous wake-up's signals for gated clock module. Also this module is responsible to synchronize the reset done information (initialization done) used by the host DMA module in order to start data transfers.

Table 78: Ports

Name	Type	Direction	Description
pi_tx_reset	wire logic	input	Transmit clock and reset Global Hardware/-Software reset (transmit clock domain, active low)
pi_tx_f_clock	wire logic	input	Transmit GMII/MII 125/25/2.5 MHz clock (from Clock Manager)
po_host_idone	reg	output	Reset done Transmit initialization done (host clock domain)
pi_host_reset	wire logic	input	Host clock and reset Global Hardware/Software reset (host clock domain, active low)
pi_host_clock	wire logic	input	Host clock (from Clock Manager)
pi_tx_stop	wire logic	input	Inputs -> Synchronized outputs Transmit stop command acknowledge (transmit clock domain)
po_host_stop	reg	output	Transmit stop command acknowledge (synchronized to host clock domain)

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Table 78 – continued from previous page

Name	Type	Direction	Description
pi_host_stop	wire logic	input	Transmit stop command (host clock domain)
po_tx_stop	reg	output	Transmit stop command (synchronized to transmit clock domain)
pi_rx_fc_tx_off	wire logic	input	Received transmit off command (receive clock domain)
po_tx_fc_tx_off	reg	output	Transmit off command (synchronized to transmit clock domain)
pi_rx_fc_xoff	wire logic	input	Receive FIFO level exceed high threshold, XOFF FC packet insert (receive clock domain)
pi_rx_fc_xon	wire logic	input	Transmit XOFF FC packet insert (synchronized to transmit clock domain)
po_tx_fc_xoff	reg	output	Receive FIFO level below low threshold, XON FC packet insert (receive clock domain)
po_tx_fc_xon	reg	output	Transmit XON FC packet insert (synchronized to transmit clock domain)

Always Blocks

`always@(posedge pi_tx_f_clock or negedge pi_tx_reset)`

Host to Transmit clock domain synchronization

`always@(posedge pi_host_clock or negedge pi_host_reset)`

Transmit to Host clock domain synchronization

Instances

ip_emac_top : *ip_emac_top*
↪mac_top : *ip_mac_top_g*
↪mac_tx_top : *ip_mac_tx_top_g*
↪tx_sync : *ip_mac_tx_sync_g*

6.41 Module ip_mac_tx_top_g

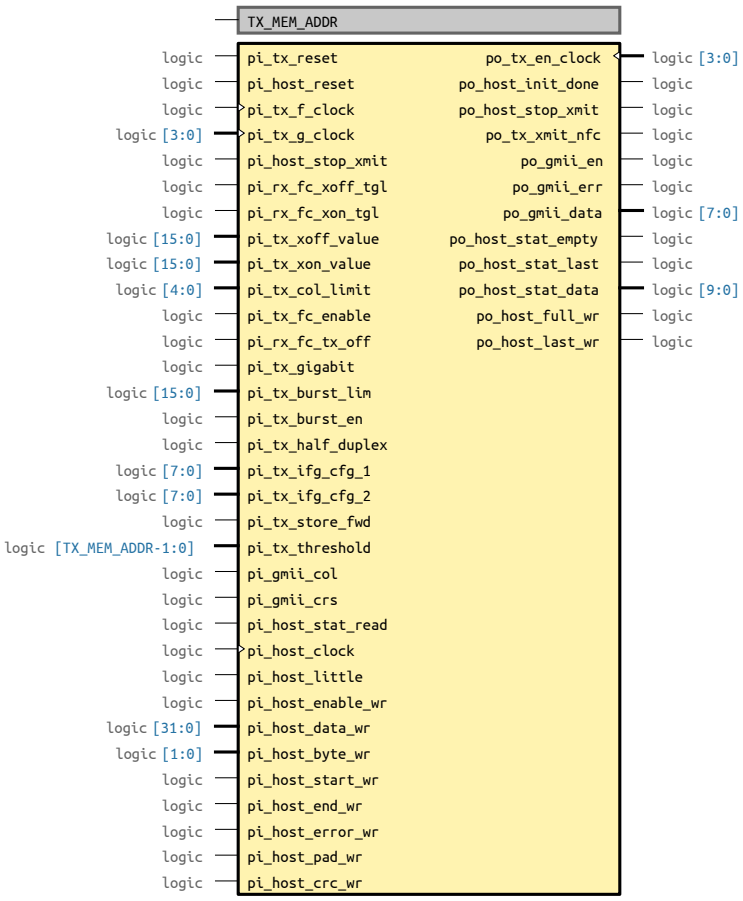

Fig. 41: Block Diagram of ip_mac_tx_top_g

Table 79: Parameters

Name	Default	Description
TX_MEM_ADDR	9	Transmit memory address width (9 -> 512 locations, 10->1024)

Table 80: Ports

Name	Type	Direction	Description
pi_tx_reset	wire logic	input	Global Software/Hardware Reset (transmit clock domain)
pi_host_reset	wire logic	input	Global Software/Hardware Reset (host clock domain)
pi_tx_f_clock	wire logic	input	Transmit clock Free Transmit GMII/MII 125/25/2.5 MHz clock (from Clock Manager)

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Table 80 – continued from previous page

Name	Type	Direction	Description
pi_tx_g_clock	wire logic [3 : 0]	input	Gated Transmit GMII/MII 125/25/2.5 MHz clock (from Clock Manager)
po_tx_en_clock	wire logic [3 : 0]	output	Enable Transmit GMII/MII 125/25/2.5 MHz clock gated clock enable
po_host_init_done	wire logic	output	Initialisation done Transmit initialisation done (host clock domain)
pi_host_stop_xmit	wire logic	input	Start/Stop transmit process Transmit EMAC stop command
po_host_stop_xmit	wire logic	output	Transmit EMAC stopped
pi_rx_fc_xoff_tgl	wire logic	input	Configuration Interface from RX EMAC insert XOFF flow control information
pi_rx_fc_xon_tgl	wire logic	input	from RX EMAC insert XON flow control information
pi_tx_xoff_value	wire logic [15 : 0]	input	from configuration XOFF flow control pause value
pi_tx_xon_value	wire logic [15 : 0]	input	from configuration XON flow control pause value
pi_tx_col_limit	wire logic [4 : 0]	input	Half Duplex back presure collision limit
pi_tx_fc_enable	wire logic	input	(maximum collision number during back presure algorithm) Transmit flow control enable
pi_rx_fc_tx_off	wire logic	input	Flow control Stop transmit commang (flow control received)
pi_tx_gigabit	wire logic	input	Operating 1000 Mbps (Gigabit) mode
pi_tx_burst_lim	wire logic [15 : 0]	input	Burst limit (valid only when operating mode is 1000 Mbps)
pi_tx_burst_en	wire logic	input	Burst enable (valid only when operating mode is 1000 Mbps)
pi_tx_half_duplex	wire logic	input	Operating Half Duplex mode
pi_tx_ifg_cfg_1	wire logic [7 : 0]	input	Interframe gap part 1 (usualy 2/3 from IFG)
pi_tx_ifg_cfg_2	wire logic [7 : 0]	input	Interframe gap part 2 (usualy 1/3 from IFG)
pi_tx_store_fwd	wire logic	input	Store and Forward transmit FIFO operating mode

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Table 80 – continued from previous page

Name	Type	Direction	Description
pi_tx_threshold	wire logic [*TX_MEM_ADDR* - 1 : 0]	input	Cut Trough (pi_emac_store_fwd not asserted) FIFO threshold
po_tx_xmit_nfc	wire logic	output	GMII/MII interface Transmit FSM data frame transmit enable (transmit clock domain)
po_gmii_en	wire logic	output	NOTE: This signal is not asserted during flow control frame transmission Transmit MII/GMII enable indication (to PHY)
po_gmii_err	wire logic	output	Transmit MII/GMII error indication (to PHY)
po_gmii_data	wire logic [7 : 0]	output	Transmit MII/GMII data (MII data is po_emac_tx_data[3:0]) (to PHY)
pi_gmii_col	wire logic	input	Collision indication (from PHY)
pi_gmii_crs	wire logic	input	Carrier Sense indication (from PHY)
pi_host_stat_read	wire logic	input	Read statistic word command
po_host_stat_empty	wire logic	output	Statistic FIFO not empty
po_host_stat_last	wire logic	output	Last statistic word indication
po_host_stat_data	wire logic [9 : 0]	output	Statistic TDES0 word data
pi_host_clock	wire logic	input	HOST interface HOST interface clock signal
pi_host_little	wire logic	input	Little endian (data path organisation)
pi_host_enable_wr	wire logic	input	Transmit MAC data path, HOST enable command
po_host_full_wr	wire logic	output	Transmit MAC data path, HOST FIFO full indication
po_host_last_wr	wire logic	output	Transmit MAC data path, HOST FIFO last location indication
pi_host_data_wr	wire logic [31 : 0]	input	Transmit MAC data path, HOST data (transmit data)
pi_host_byte_wr	wire logic [1 : 0]	input	Transmit MAC data path, HOST byte enable (transmit data byte enable)
pi_host_start_wr	wire logic	input	Transmit MAC data path, HOST start of frame indication

continues on next page

Table 80 – continued from previous page

Name	Type	Direction	Description
pi_host_end_wr	wire logic	input	Transmit MAC data path, HOST start of frame indication
pi_host_error_wr	wire logic	input	Unused please check if useful (if not remove)
pi_host_pad_wr	wire logic	input	Transmit MAC data path, HOST padding enable (valid only when pi_host_end_wr)
pi_host_crc_wr	wire logic	input	Transmit MAC data path, HOST crc enable (valid only when pi_host_end_wr)

Instances

ip_emac_top : *ip_emac_top*
↪mac_top : *ip_mac_top_g*
↪mac_tx_top : *ip_mac_tx_top_g* #(.TX_MEM_ADDR(10))

Submodules

ip_mac_tx_top_g #(.TX_MEM_ADDR(10))
↪tx_bkoff : *ip_mac_tx_bkoff_g*
↪tx_data_async : *ip_async_fifo_g* #(.MEM_WIDTH(39))
↪tx_data_dram : *ip_mac_dram_001* #(.MEM_ADDR(10), .MEM_WIDTH(39))
↪tx_dpath : *ip_mac_tx_dpath_g*
↪tx_dsplit : *ip_mac_tx_dsplit_g* #(.MEM_ADDR(10))
↪tx_endian : *ip_mac_big_endian*
↪tx_fc_gen : *ip_mac_fc_gen_g*
↪tx_fifo : *ip_mac_tx_fifo_g* #(.MEM_ADDR(10))
↪tx_fsm : *ip_mac_tx_fsm_g*
↪tx_gmii : *ip_mac_tx_gmii_g*
↪tx_stat_async : *ip_async_fifo_g* #(.MEM_WIDTH(10))
↪tx_sync : *ip_mac_tx_sync_g*

6.42 Module ip_sync_cell

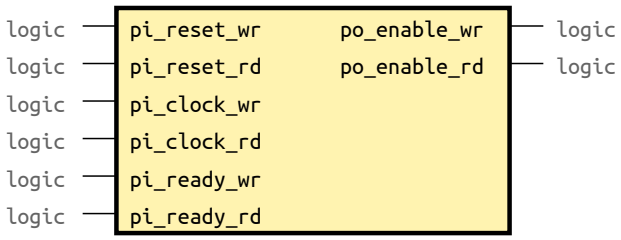

Fig. 42: Block Diagram of ip_sync_cell

Overview

The synchronization cell is responsible for the write/read enable signals synchronization. The write enable signal indicates that a new write clock domain data can be synchronized to the read clock domain. The read enable signal indicates that the external data can be safely read on the read clock domain.

Table 81: Ports

Name	Type	Direction	Description
pi_reset_wr	wire logic	input	reset write clock domain (synchronous)
pi_reset_rd	wire logic	input	reset read clock domain (synchronous)
pi_clock_wr	wire logic	input	write clock
pi_clock_rd	wire logic	input	read clock
po_enable_wr	wire logic	output	write enable (combinatorial output)
po_enable_rd	wire logic	output	read enable (combinatorial output)
pi_ready_wr	wire logic	input	write ready (data available for write)
pi_ready_rd	wire logic	input	read ready (data available for read)

Always Blocks

`always@(posedge pi_clock_rd or negedge pi_reset_rd)`

syncronized toggle write (synchronization second DFF)

`always@(posedge pi_clock_wr or negedge pi_reset_wr)`

syncronized toggle read (synchronization second DFF)

Instances

ip_emac_top : *ip_emac_top*
↪mac_top : *ip_mac_top_g*
↪mac_rx_top : *ip_mac_rx_top_g*
↪rx_async : *ip_async_fifo_g*
↪cell_0 : *ip_sync_cell*
↪cell_1 : *ip_sync_cell*

↪cell_2 : *ip_sync_cell*
↪cell_3 : *ip_sync_cell*
↪cell_4 : *ip_sync_cell*
↪cell_5 : *ip_sync_cell*
↪cell_6 : *ip_sync_cell*
↪cell_7 : *ip_sync_cell*
↪mac_tx_top : *ip_mac_tx_top_g*
↪tx_data_async : *ip_async_fifo_g*
↪cell_0 : *ip_sync_cell*
↪cell_1 : *ip_sync_cell*
↪cell_2 : *ip_sync_cell*
↪cell_3 : *ip_sync_cell*
↪cell_4 : *ip_sync_cell*
↪cell_5 : *ip_sync_cell*
↪cell_6 : *ip_sync_cell*
↪cell_7 : *ip_sync_cell*
↪tx_stat_async : *ip_async_fifo_g*
↪cell_0 : *ip_sync_cell*
↪cell_1 : *ip_sync_cell*
↪cell_2 : *ip_sync_cell*
↪cell_3 : *ip_sync_cell*
↪cell_4 : *ip_sync_cell*
↪cell_5 : *ip_sync_cell*
↪cell_6 : *ip_sync_cell*
↪cell_7 : *ip_sync_cell*

Submodules

ip_sync_cell
↪metastable_toggle_rd : *dff_metastable* #(.DFF_WIDTH(1))
↪metastable_toggle_wr : *dff_metastable* #(.DFF_WIDTH(1))

6.43 Module ip_sync_reset_g

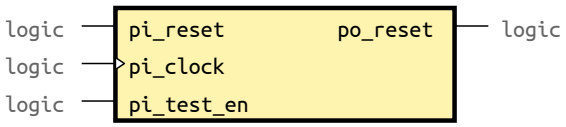

Fig. 43: Block Diagram of ip_sync_reset_g

Overview

Synchronous resets are used in designs to safely reset the DFFs from one clock domain. The asynchronous reset can generate an unstable condition in design due to the metastability when reset is removed, if the DFF input data is different than the reset value output DFF data (for example a free counter)

Table 82: Ports

Name	Type	Direction	Description
pi_reset	wire logic	input	Asynchronous reset
pi_clock	wire logic	input	Input clock
pi_test_en	wire logic	input	Test enable (multiplex information)
po_reset	wire logic	output	Synchronous reset (functional clock balanced)

Always Blocks

`always@(posedge pi_clock or negedge pi_reset)`

Metastable Reset Synchronization

Instances

ip_emac_top : *ip_emac_top*
- ↪host_clk_mng : *ip_host_clk_mng_g*
  - ↪host_sreset : *ip_sync_reset_g*
  - ↪hw_host_sreset : *ip_sync_reset_g*
- ↪mac_top : *ip_mac_top_g*
  - ↪mac_clk_mng : *ip_mac_clk_mng_g*
    - ↪host_sreset : *ip_sync_reset_g*
    - ↪hw_host_sreset : *ip_sync_reset_g*
    - ↪mdio_sreset : *ip_sync_reset_g*
    - ↪rx_sreset : *ip_sync_reset_g*
    - ↪tx_sreset : *ip_sync_reset_g*

6.44 Module ip_synchronous_fifo

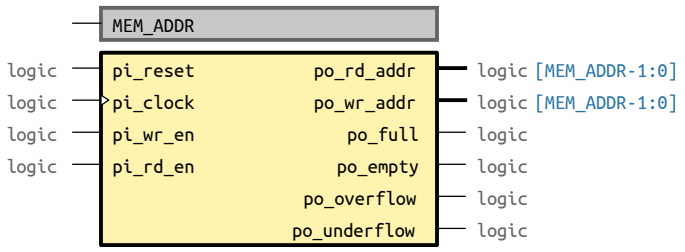

Fig. 44: Block Diagram of ip_synchronous_fifo

Table 83: Parameters

Name	Default	Description
MEM_ADDR	6	Transmit memory address width (9 -> 512 locations, 10->1024)

Table 84: Ports

Name	Type	Direction	Description
pi_reset	wire logic	input	
pi_clock	wire logic	input	
po_rd_addr	wire logic [*MEM_ADDR* - 1 : 0]	output	
po_wr_addr	wire logic [*MEM_ADDR* - 1 : 0]	output	
pi_wr_en	wire logic	input	
pi_rd_en	wire logic	input	
po_full	wire logic	output	
po_empty	wire logic	output	
po_overflow	wire logic	output	
po_underflow	wire logic	output	

Always Blocks

`always@(posedge pi_clock or negedge pi_reset)`

Read Address Update Process

`always@(posedge pi_clock or negedge pi_reset)`

Write Address Update Process

CHAPTER
SEVEN

MACROS

Table 1: Defined Control Defines

Name	Description
SIMULATION_VALUE_REDUCED	synopsys translate_off Reduced 512 time slot (for simulation)

Table 2: Undefined Control Defines

Name	Description
EMAC_10_100_MBPS	

Table 3: Defines

Name	Value	Description
AE_BIT	2	
ARB_IDLE	3'b000	ARBITER states
ARB_RX	3'b010	
ARB_RX_DS	3'b100	
ARB_S0	3'b001	
ARB_TX	3'b011	
ARB_TX_DS	3'b101	
ARB_TX_UPD	3'b110	
BF_BIT	9	
BK_DONE	1'b1	Backoff DONE state (wait slot_cnt tobe equal bk_ended value)
BK_IDLE	1'b0	Backoff IDLE state (wait for pi_bk_start command)
CC_BIT	5:2	
CDID_DEVICE_TYPE	16'h3030	
CE_BIT	1	
CFID_MAC_ID	16'h1010	
CFID_MANUFACTURER_ID	16'h2020	
DATA	3'h7	
DATA_DROP	3'h2	
DATA_READ	3'h1	
DEVADDR	3'h4	
DE_BIT	0	
EC_BIT	6	
EF_BIT	4	
ERROR_LENGTH	8'h04	
FC_DEST_ADDR	48'h0180C2000001	Control frame destination address
FC_IDLE	2'd0	FSM states encoding (flow control frame FSM)
FC_OP_TYPE	2'd1	
FC_READ	3'h4	
FC_TIME_VAL	2'd2	
FC_WAIT_64	2'd3	
FL_BIT	22:8	Statistic word bits

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Table 3 – continued from previous page

Name	Value	Description
HASH	3'd2	
HOST_NOP	2'b00	
HOST_READ	2'b10	HOST bus interface operations
HOST_WRITE	2'b01	
IDLE	3'd0	FSM States And Control Data Define *
LC_BIT	7	
LE_BIT	3	
LP_BIT	7	
MATCH_1	3'd3	
MATCH_2	3'd4	
MF_BIT	6	
MULTICAST_BIT	40	Global multicast bit (see 802.3-2002_part2.pdf, 22.2.3 Frame structure)
OF_BIT	0	
OPCODE	3'h3	
PREAMBLE	3'h1	
REGADDR	3'h5	
REGS_HWRITE	3'b100	
REGS_IDLE	3'b000	
REGS_READ	3'b010	
REGS_WRITE	3'b001	
RX_CRC_CHECK	32'hC704DD7B	CRC check value
RX_DA	4'h3	
RX_DATA_0	4'h6	
RX_DATA_1	4'h7	
RX_DS_IDLE	3'b000	RX ds aquire state values
RX_DS_MAIN	3'b001	
RX_DS_READ	3'b010	
RX_DS_SUSPEND	3'b011	
RX_DS_WAIT	3'b100	
RX_ERROR_DATA	8'h1f	
RX_EXTEND	4'h8	
RX_EXTEND_DATA	8'h0f	
RX_FCOPTYPE_CHECK_0	8'h88	FC frame opcode
RX_FCOPTYPE_CHECK_1	8'h08	
RX_FCOPTYPE_CHECK_2	8'h00	
RX_FCOPTYPE_CHECK_3	8'h01	
RX_IDLE	4'h0	FSM states encoding (receive frame)
RX_PREAMBLE	4'h1	
RX_PREAMBLE_DATA	4'h5	GMII Data encoding
RX_READ_DS	3'b001	
RX_SA	4'h4	
RX_SFD	4'h2	
RX_SFD_DATA	4'hd	
RX_STAT	3'b101	
RX_TYPE	4'h5	
RX_WAIT	4'h9	
RX_WRITE	3'b011	
RX_WRITE_DS	3'b110	
RX_WRITE_PAUSE	3'b010	
SPLIT_IDLE	3'h0	FSM states encoding
SPLIT_WAIT	3'h3	
START	3'h2	

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Table 3 – continued from previous page

Name	Value	Description
TJ_BIT	8	
TL_BIT	5	
TP	1	Delay assertion output signals
TURNAR	3'h6	
TX_BACKOFF	4'h8	
TX_BEGIN	4'd0	Defer State Coding * Transmit IFG initialize after reset (only)
TX_CARRIER	4'd7	Carrier monitor (after remote transmit)
TX_CRC	4'h6	
TX_CRS_ERR	4'hd	
TX_CRS_JAM	4'hc	
TX_DATA	4'h4	
TX_DEFER	4'h1	
TX_DS_IDLE	3'b000	TX ds aquire state values
TX_DS_MAIN	3'b001	
TX_DS_READ	3'b010	
TX_DS_SUSPEND	3'b011	
TX_DS_UPD_IDLE	2'b00	
TX_DS_UPD_WRITE	2'b01	
TX_DS_WAIT	3'b100	
TX_ERROR	4'd3	Collision during carrier extend phase
TX_ERROR_DATA	8'h1f	
TX_EXTEND	4'h9	
TX_EXTEND_DATA	4'hf	
TX_IDLE	4'd1	Transmit enable
TX_IDLE_DATA	8'h00	
TX_IFG1	4'd5	IFG1 (ignore the carrier sense assertion)
TX_IFG2	4'd6	IFG2 (ignore the carrier sense assertion)
TX_JAM	4'd2	Collision during data phase
TX_JAM_DATA	4'hf	
TX_JAM_NIBBLE	4'hf	
TX_LATENCY	4'd8	MAC latency 2 cycles
TX_LW_BUFF	4'b1000	
TX_LW_BURST	4'b1001	
TX_LW_DS	4'b0111	
TX_LW_FRM	4'b0110	
TX_MAC_JABBER_WORDS_-LIMIT	16'h1001	
TX_PAD	4'h5	
TX_PAD_DATA	4'h0	
TX_PREAMBLE	4'h2	
TX_PREAMBLE_DATA	4'h5	
TX_READ	4'b0011	
TX_READ_DS	4'b0001	
TX_READ_PAUSE	4'b0010	
TX_SFD	4'h3	
TX_SFD_DATA	4'hd	
TX_STOP	4'hb	
TX_UPD_FIFO_RANGE	3	Range of the tx descriptor update fifo =log2(&96;TX_UPD_FIFO_SIZE)

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Table 3 – continued from previous page

Name	Value	Description
TX_UPD_FIFO_SIZE	8	Size of the tx descriptor update fifo
TX_UPD_WAIT	4'b0101	
TX_WAIT	4'd4	Wait carrier to be deasserted after own transmit
TX_WRITE_DS	4'b0100	
UF_BIT	1	
WAIT	3'd1	
WRITE_1	3'd1	Write table (write odd word)
WRITE_2	3'd2	and exact address match 16-bits (when last Hash + 1 Exact Address Match) Write table exact address match 16-bits (1 Exact Address Match)
WRITE_3	3'd3	Write table exact address match 16-bits (1 Exact Address Match)
WRITE_4	3'd4	Write table exact address match 16-bits (1 Exact Address Match)
WR_DATA	3'd1	
WR_EXTEND	3'd4	
WR_IDLE	3'd0	FSM states encoding (memory write FSM)
WR_OVERRUN	3'd2	
WR_STAT	3'd3	